EE 330

Lecture 35

Amplifier Biasing

Frequency-Dependent Performance of Amplifiers

Parasitic Capacitances in MOS Devices

Exam Schedule

Exam 1	Friday Sept 24
Exam 2	Friday Oct 22
Exam 3	Friday Nov 19
Final	Tues Dec 14 12:00 p.m.

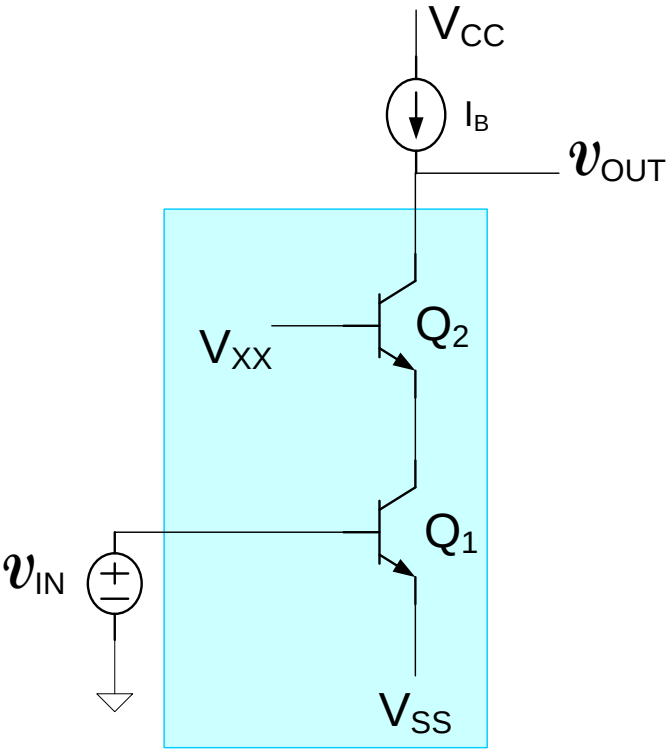
As a courtesy to fellow classmates, TAs, and the instructor

Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

Review from Last Lecture

Cascode Configuration

Discuss



$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{02}}\beta\right] \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$

$$g_{0CC} \cong \frac{g_{02}}{\beta}$$

$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta = \left[\frac{2V_{AF}}{V_t}\right]\beta = [-8000]100$$

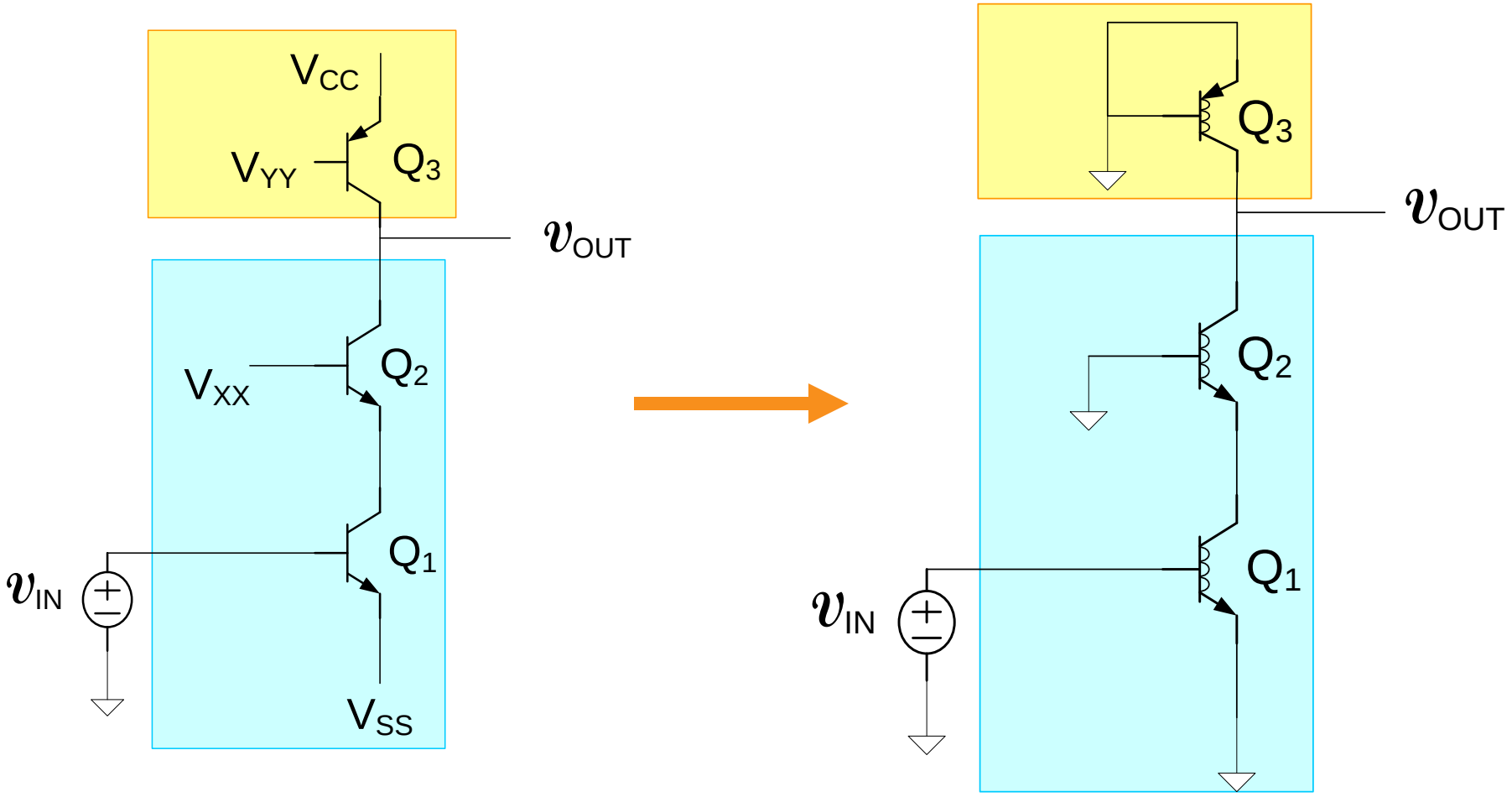
$$A_{VCC} \cong -800{,}000$$

This gain is very large and only requires two transistors!

What happens to the gain if a transistor-level current source is used for I_B?

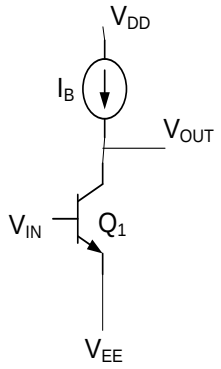
Review from Last Lecture

Cascode Configuration

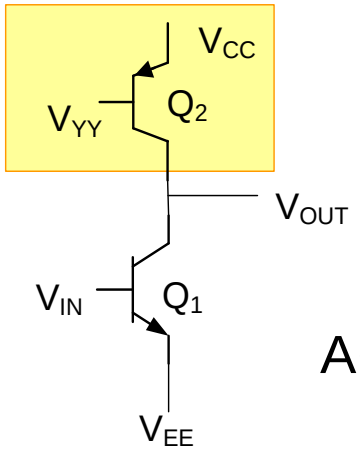


Review from Last Lecture

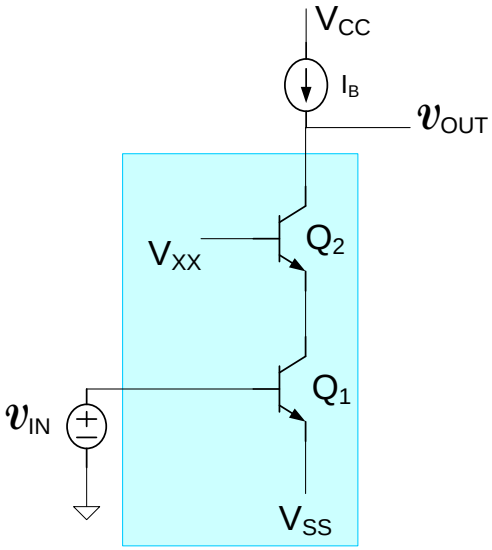
Cascode Configuration Comparisons



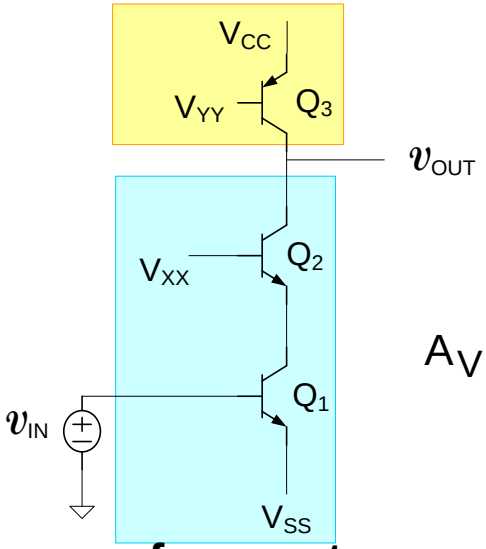
$$A_V = \frac{-g_m}{g_0}$$



$$A_V \cong \frac{-g_{m1}}{g_{01}+g_{02}} = \frac{-g_{m1}}{2g_{01}}$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$



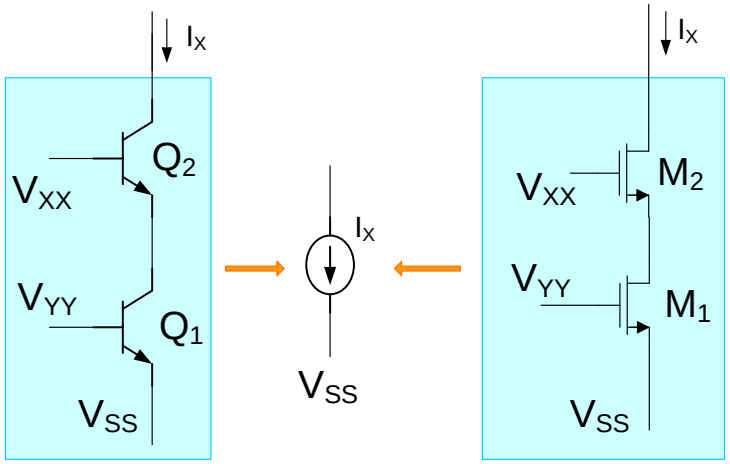
$$A_V \cong -\left[\frac{g_{m1}}{\frac{g_{01}}{\beta}+g_{03}}\right] \cong -\left[\frac{g_{m1}}{g_{03}}\right]$$

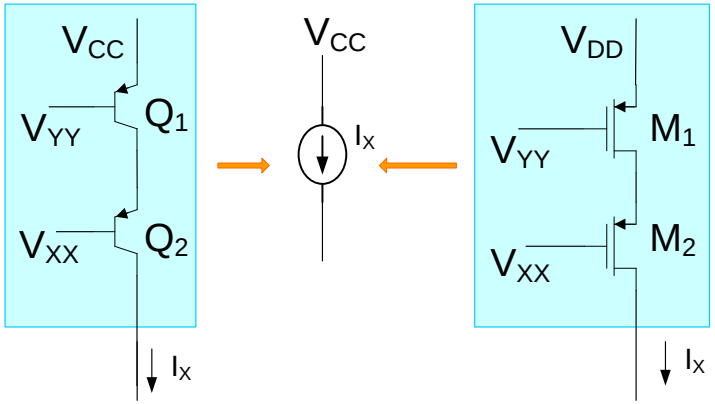
Gain limited by output impedance of current scource !!

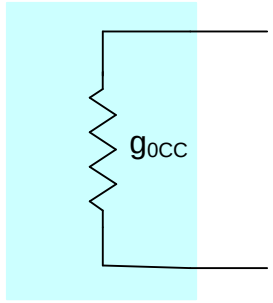
Can we design a better current source?

In particular, one with a higher output impedance?

Cascode current sources







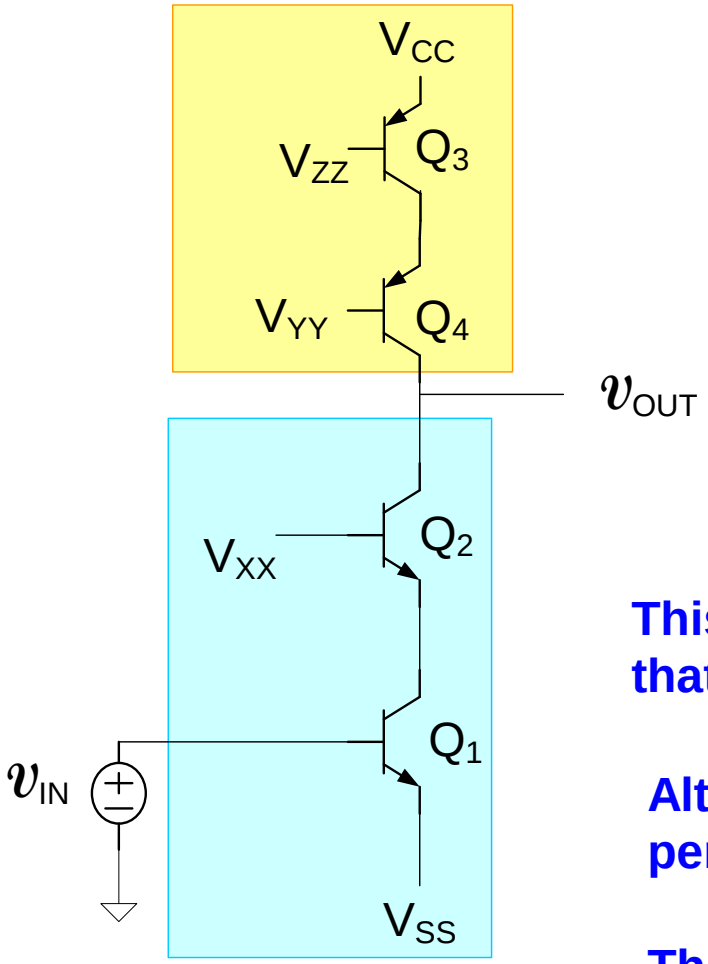
All have the same small-signal model

$$g_{OCC} = \left[\frac{g_{02}\left(g_{01}+g_{\pi 2}\right)}{g_{01}+g_{02}+g_{\pi 2}+g_{m2}} \right]$$

Review from Last Lecture

Cascode Configuration

Discuss



$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right]\frac{\beta}{2}$$

$$A_V = -[8000]\frac{100}{2} \cong -400{,}000$$

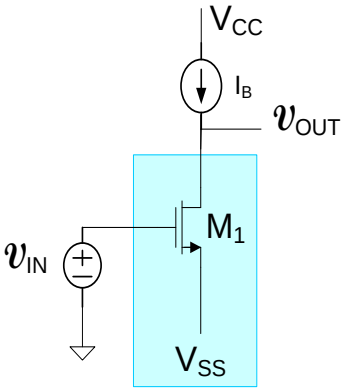
This gain is very large and is a factor of 2 below that obtained with an ideal current source biasing

Although the factor of 2 is not desired, the performance of this circuit is still very good

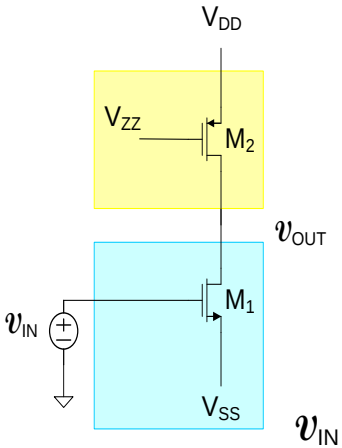
This factor of 2 gain reduction is that same as was observed for the CE amplifier when a transistor-level current source was used

Review from Last Lecture

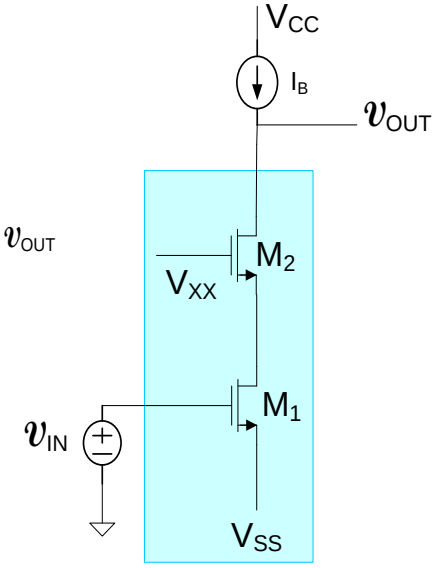
High Gain Amplifier Comparisons (n-ch MOS)



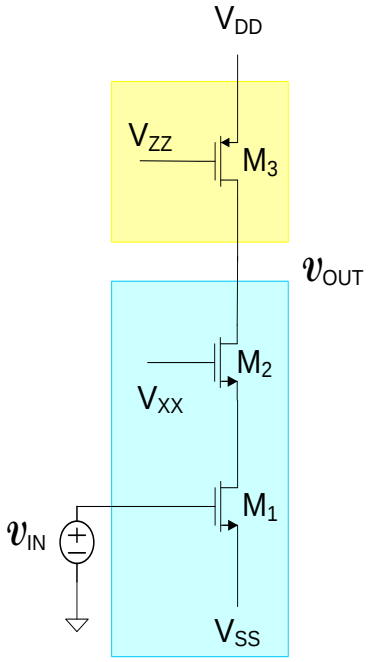
$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$



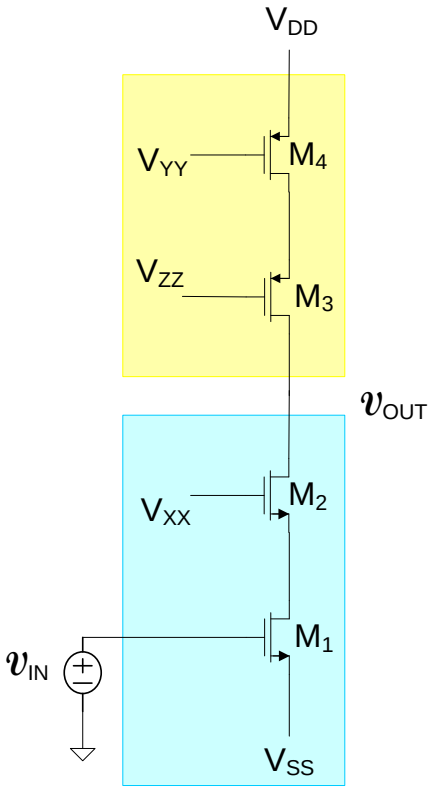
$$A_V \cong -\frac{1}{2}\left[\frac{g_{m1}}{g_{01}}\right]$$



$$A_{VCC} \cong -\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$



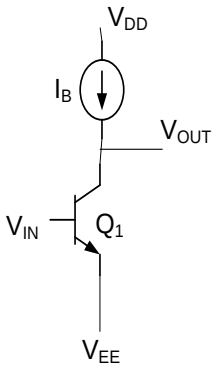
$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$



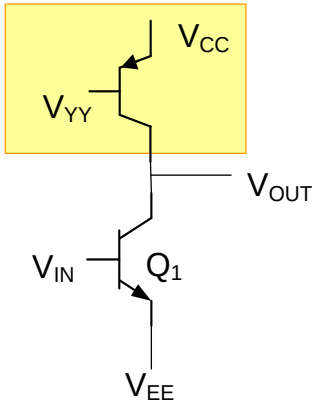
$$A_{VCC} \cong -\frac{1}{2}\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$

Review from Last Lecture

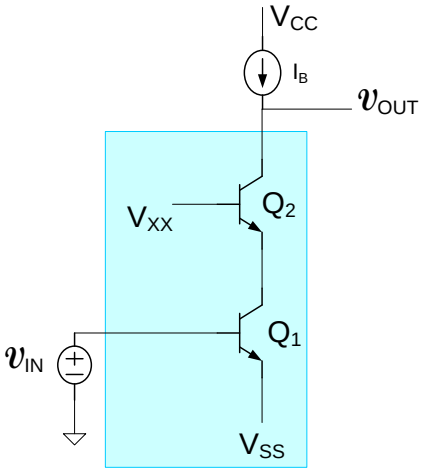
High Gain Amplifier Comparisons (BJT)



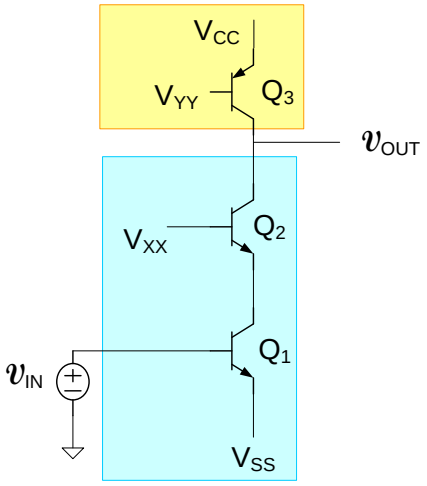
$$A_V = \frac{-g_m}{g_0}$$



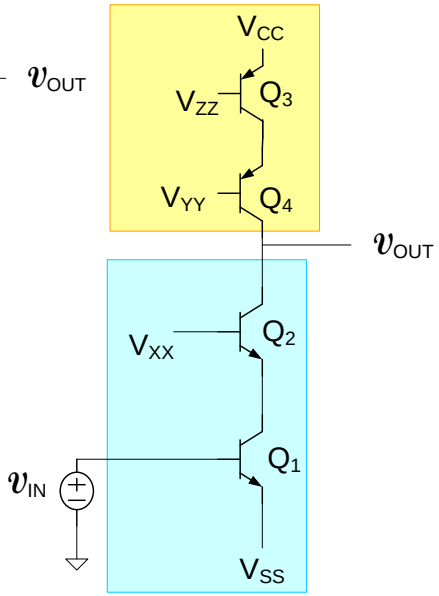
$$A_V \cong -\frac{1}{2}\frac{g_{m1}}{g_{01}}$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$



$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right]\frac{\beta}{2}$$

- Single-ended high-gain amplifiers inherently difficult to bias (because of the high gain)
- Biasing becomes practical when used in differential applications
- These structures are widely used but usually with differential inputs

Amplifier Biasing

Amplifier biasing is that part of the design of a circuit that establishes the desired operating point (or Q-point)

Goal is to invariably minimize the impact the biasing circuit has on the small-signal performance of a circuit

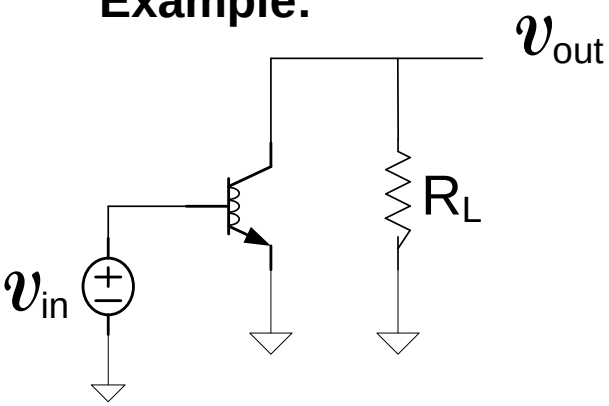
Usually at most 2 dc power supplies are available and these are often fixed in value by system requirements – this restriction is cost driven

Discrete amplifiers invariable involve adding biasing resistors and use capacitor coupling and bypassing

Integrated amplifiers often use current sources which can be used in very large numbers and are very inexpensive

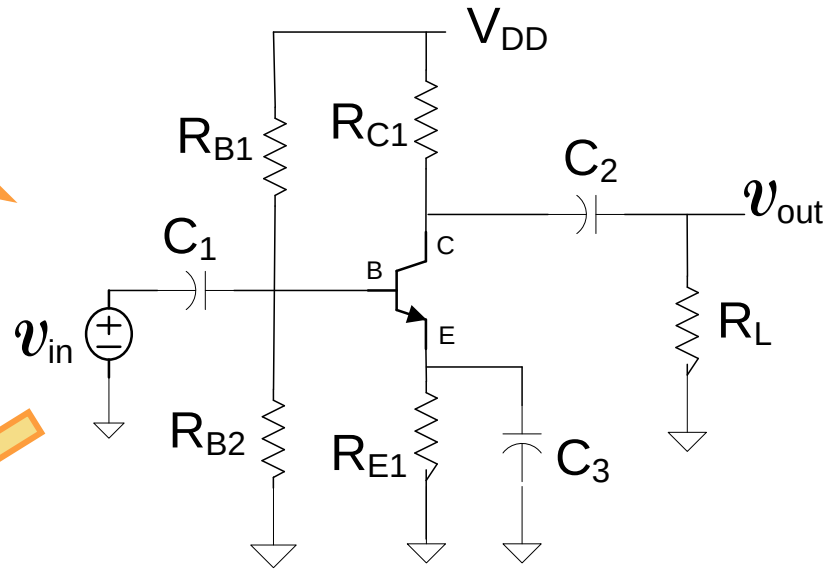
Amplifier Biasing

Example:

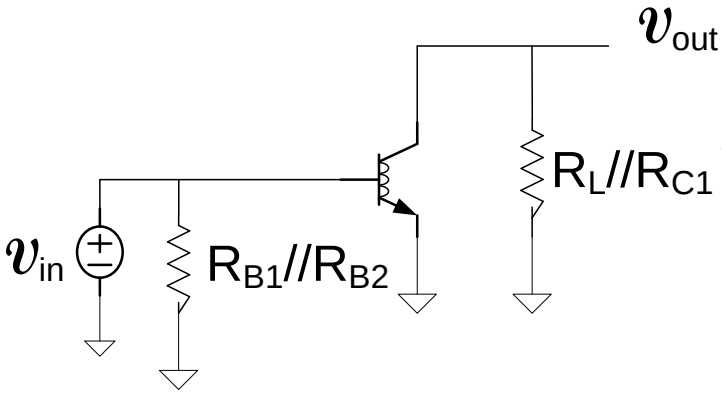


$$A_V = -g_m R_L$$

Desired small-signal circuit
Common Emitter Amplifier



Biased circuit

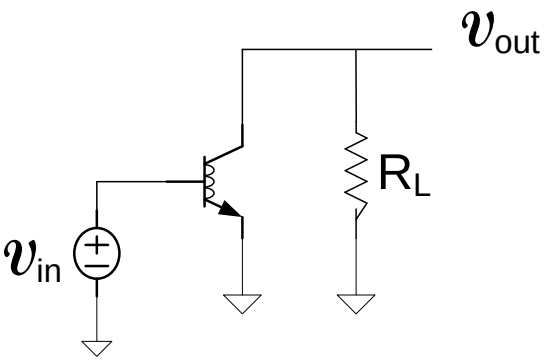


Actual small-signal circuit

$$A_V = -g_m \left(R_L // R_{C1} \right)$$

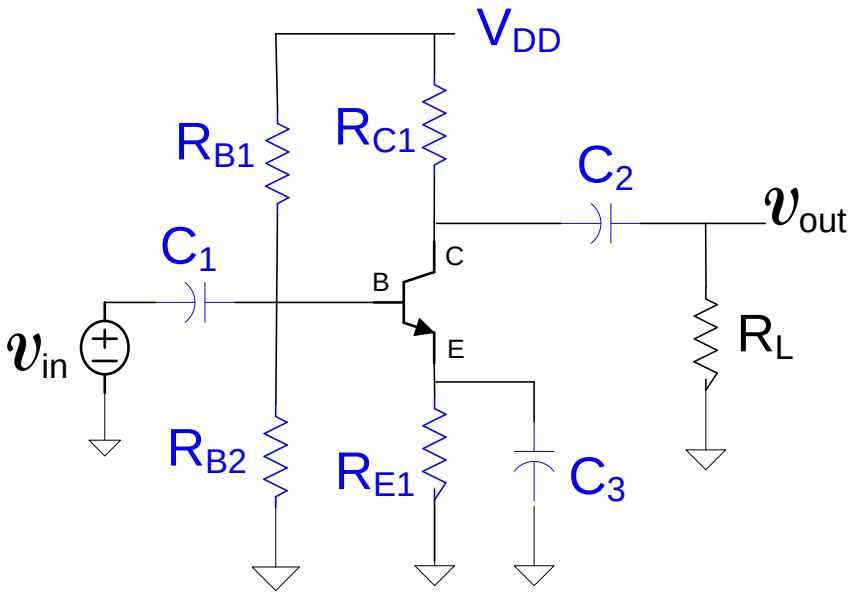
Amplifier Biasing

Example:



Desired small-signal circuit
Common Emitter Amplifier

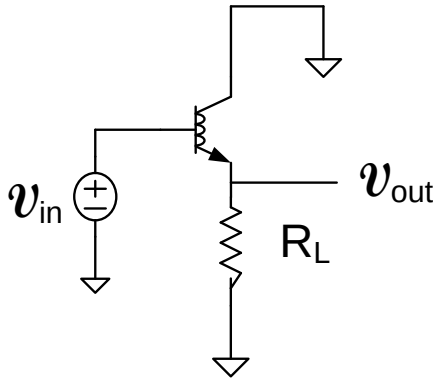
Biasing components shown in blue



Biased small-signal circuit

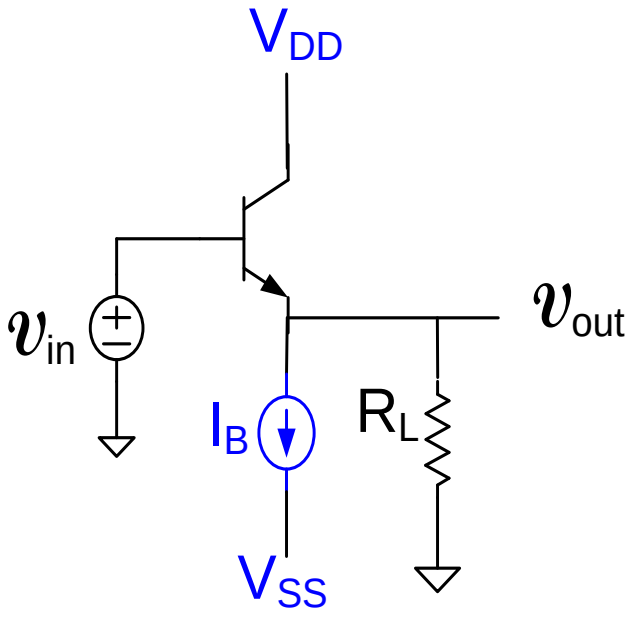
Amplifier Biasing

Example:



Desired small-signal circuit
Common Collector Amplifier

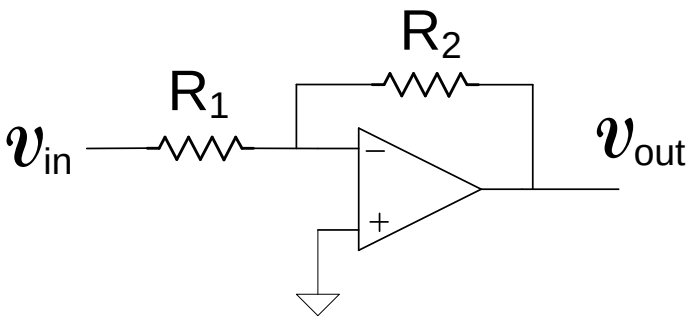
Biasing components shown in blue



Biased circuit

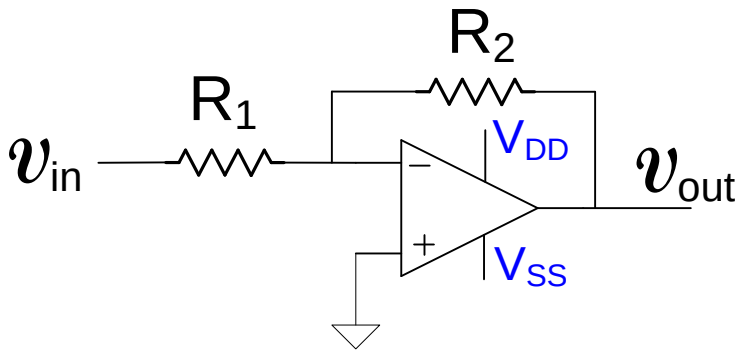
Amplifier Biasing

Example:



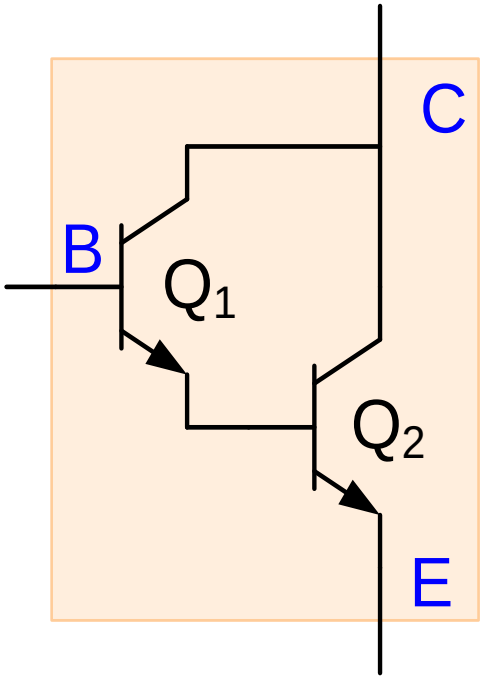
Desired small-signal circuit
Inverting Feedback Amplifier

Biasing components shown in blue

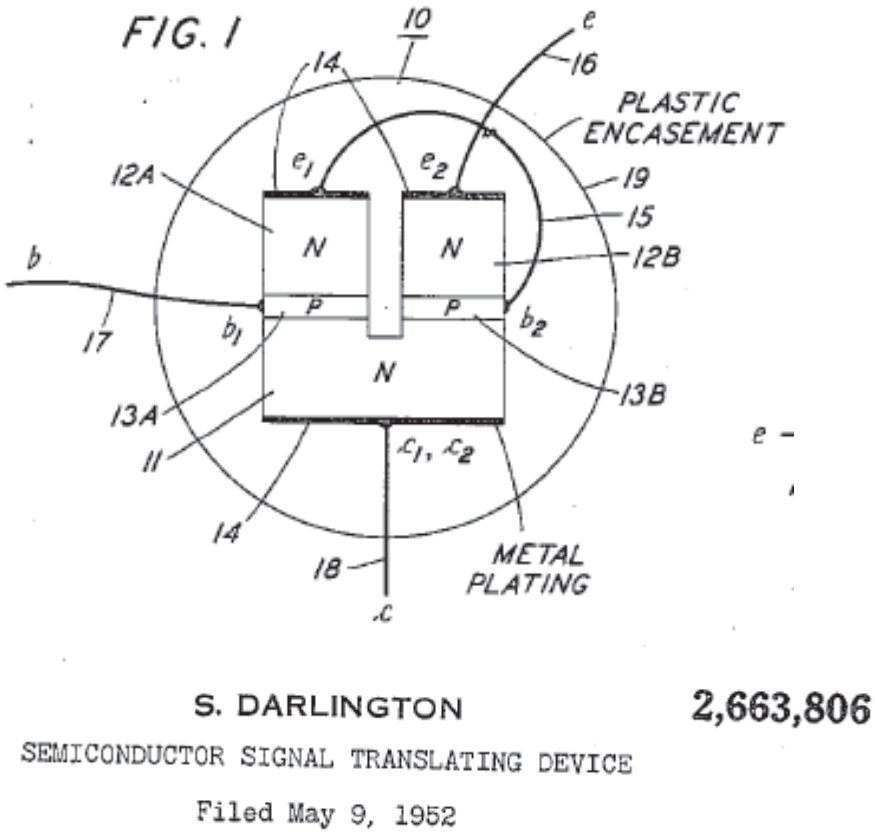


Biased circuit

Other Basic Configurations

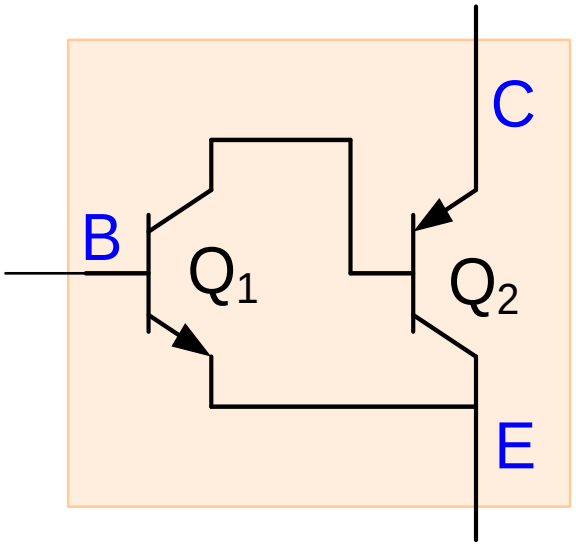


Darlington Configuration



- **Current gain is approximately β^2**
- **Two diode drop between B_{eff} and E_{eff}**

Other Basic Configurations



Sziklai Pair

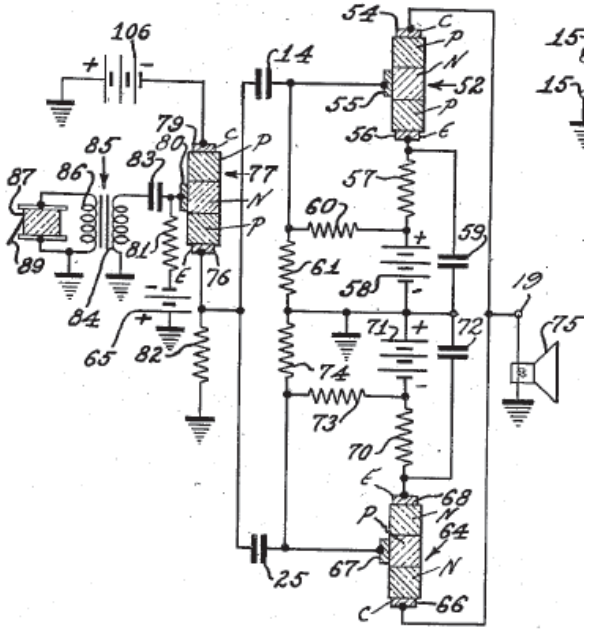


FIG. 3.

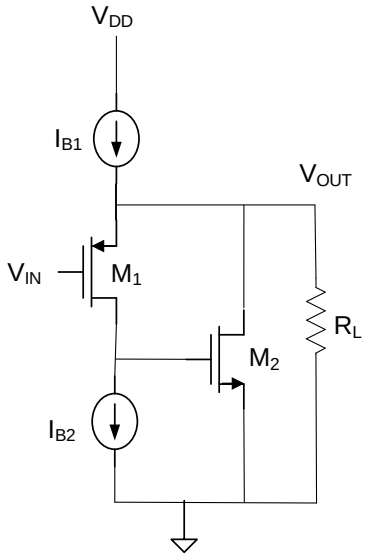
May 7, 1957 G. C. SZIKLAI 2,791,644

PUSH-PULL AMPLIFIER WITH COMPLEMENTARY TYPE TRANSISTORS

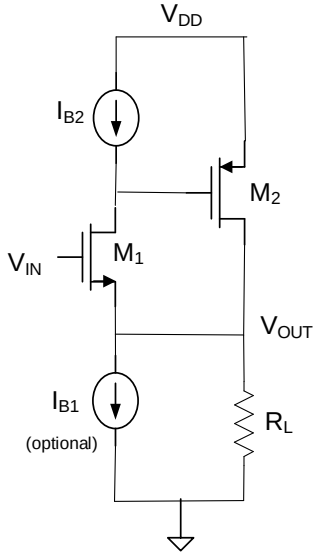
Filed Nov. 7, 1952

- **Gain similar to that of Darlington Pair**
- **Current gain is approximately $\beta_n \beta_p$**
- **Current gain will not be as large when $\beta_p < \beta_n$**
- **Only one diode drop between B_{eff} and E_{eff}**

Other Basic Configurations



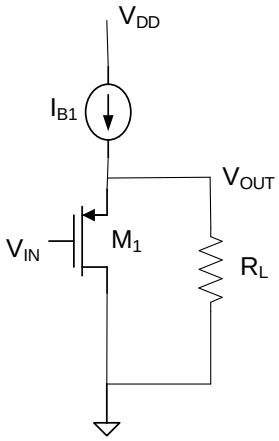
(c)



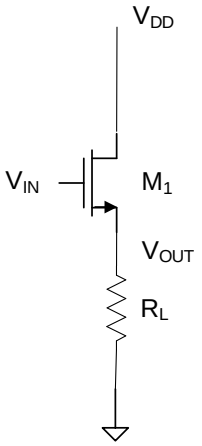
(d)

Buffer and Super Buffer

- Voltage shift varies with V_{IN} in buffer
- Current through shift transistor is constant for Super Buffer as V_{IN} changes so voltage shift does not change with V_{IN}
- Same nominal voltage shift



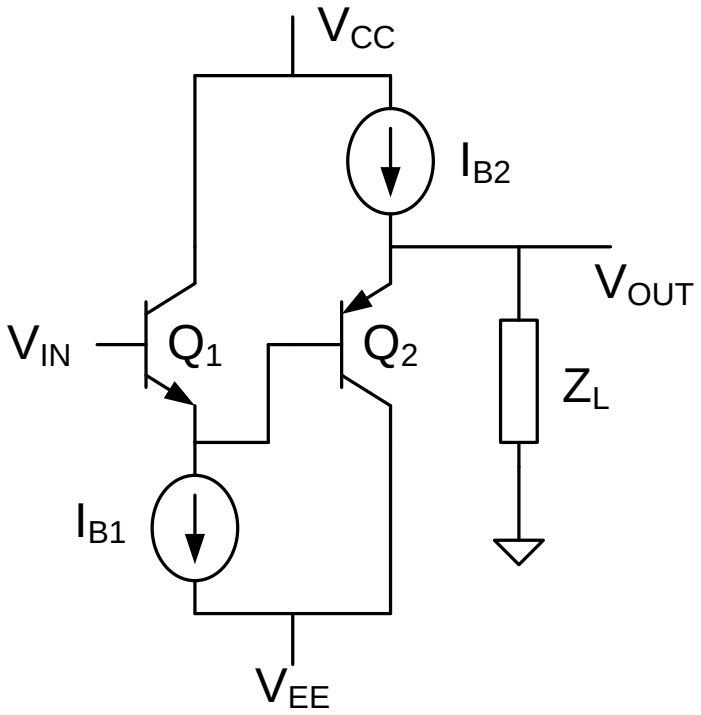
(a)

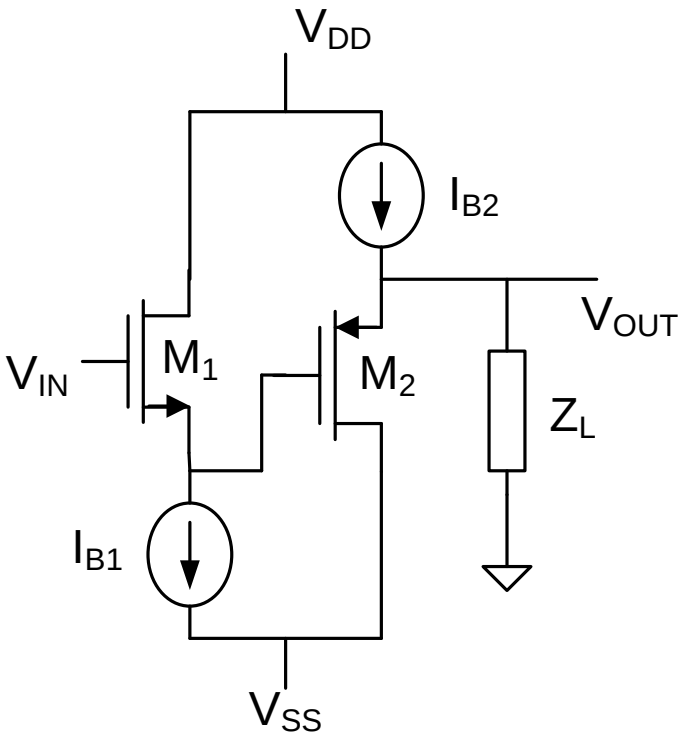


(b)

Other Basic Configurations

Low offset buffers

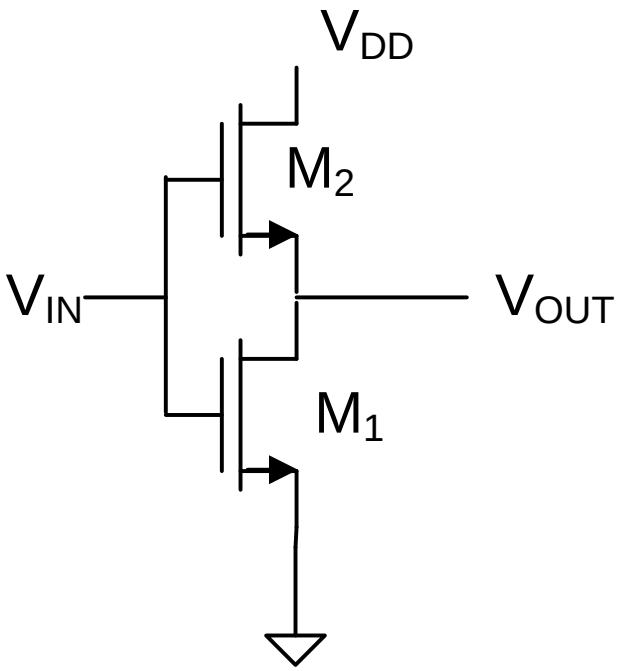


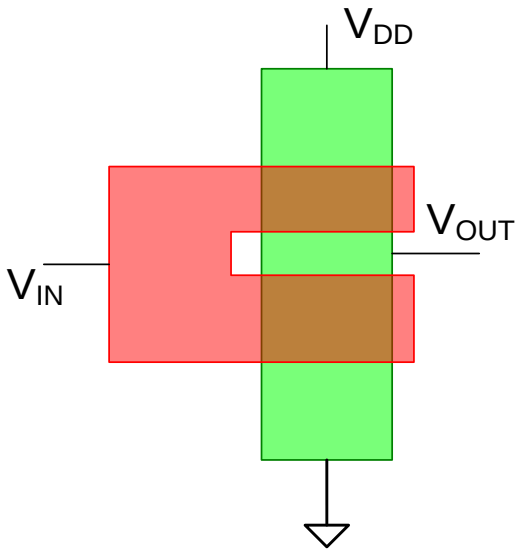


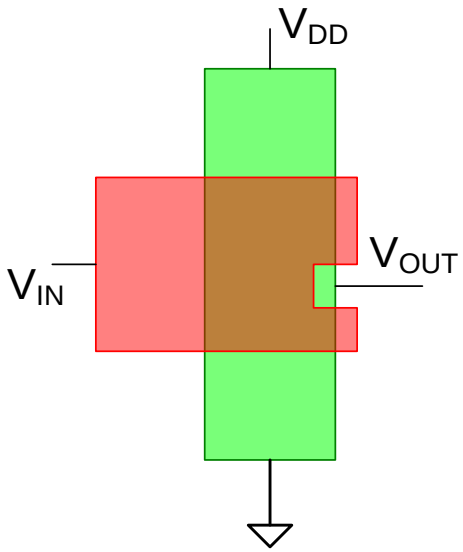
- **Actually a CC-CC or a CD-CD cascade**
- **Significant drop in offset between input and output**
- **Biasing with DC current sources**
- **Can Add Super Buffer to Output**

Other Basic Configurations

Voltage Attenuator



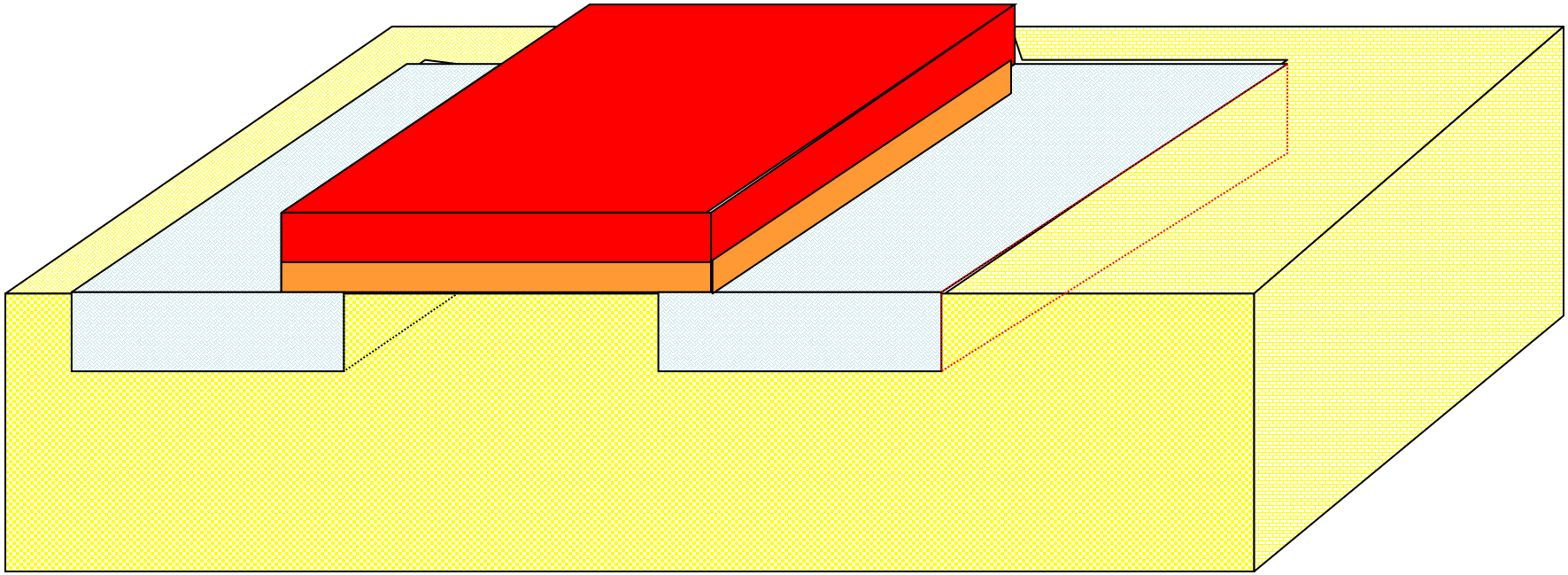




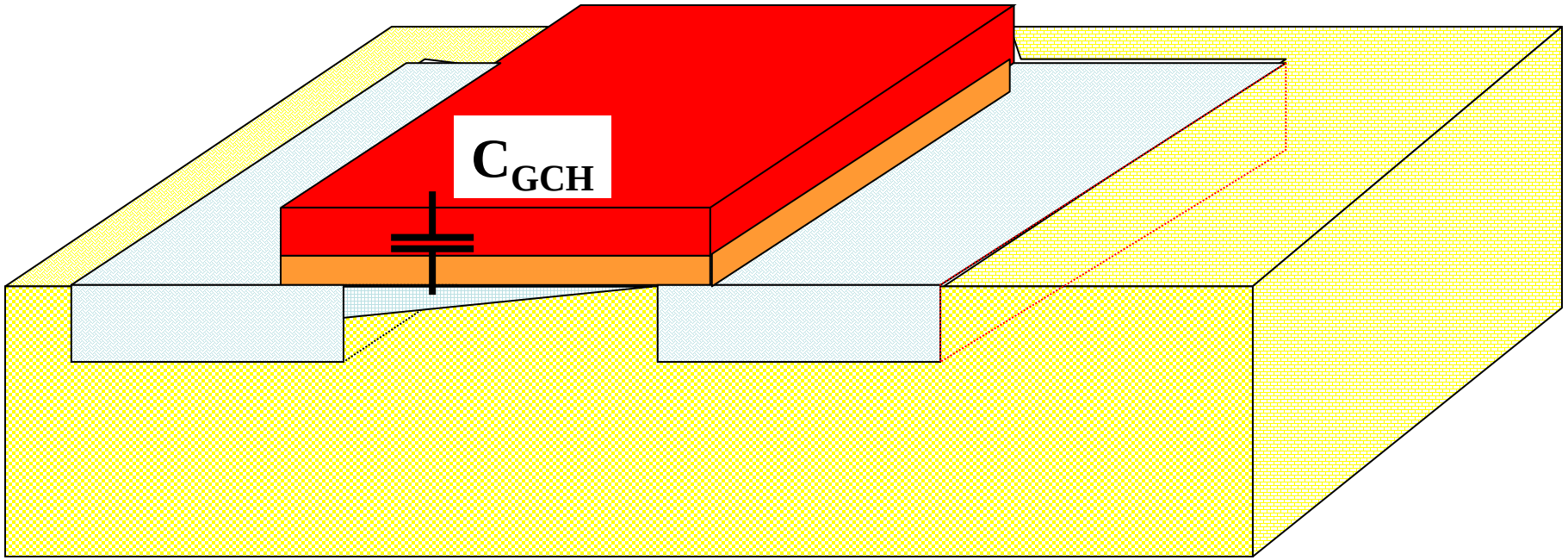
- **Attenuation factor is quite accurate (Determined by geometry)**
- **Infinite input impedance**
- **M_1 in triode, M_2 in saturation**
- **Actually can be a channel-tapped structure**

Frequency-Dependent Performance of Amplifiers

Parasitic Capacitors in MOSFET

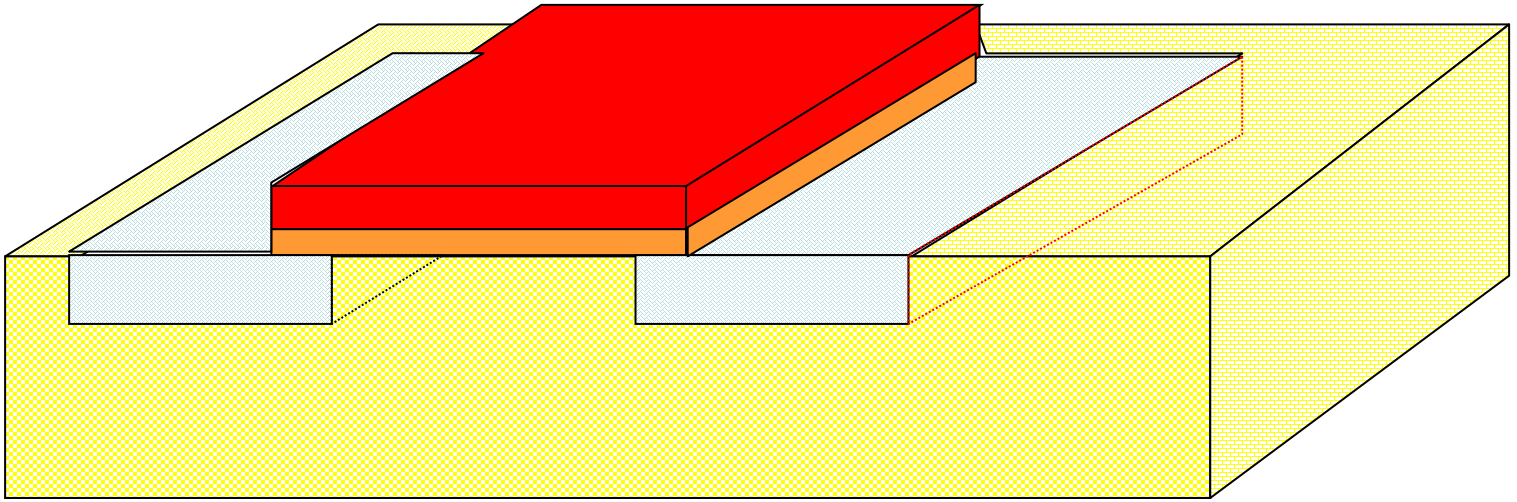


Parasitic Capacitors in MOSFET

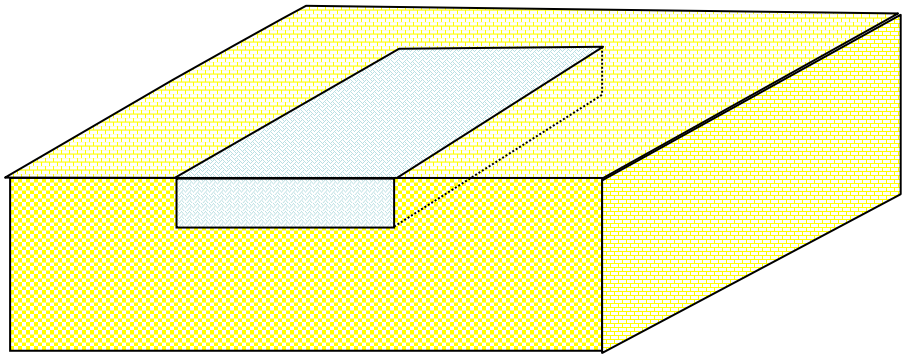


- This capacitance was modeled previously and exists when the transistor is operating in triode or saturation
- But there are others that also affect high-frequency or high-speed operation

Parasitic Capacitors in MOSFET

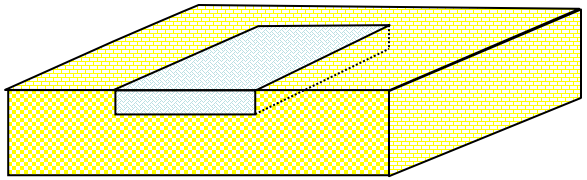


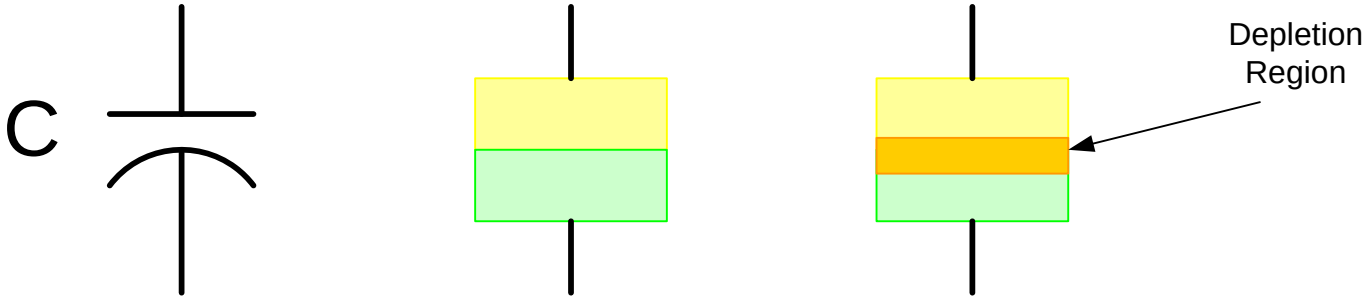
Recall that pn junctions have a depletion region!



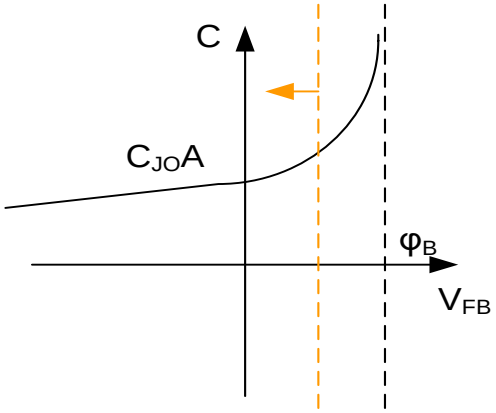
Parasitic Capacitors in MOSFET

pn junction capacitance





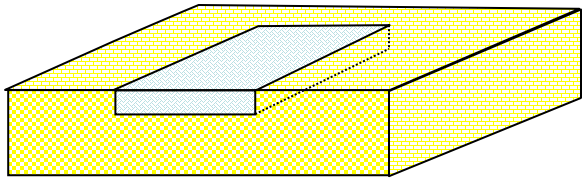
For $V_{FB}<\varphi_B/2$



$$C = \frac{C_{J0} A}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

Parasitic Capacitors in MOSFET

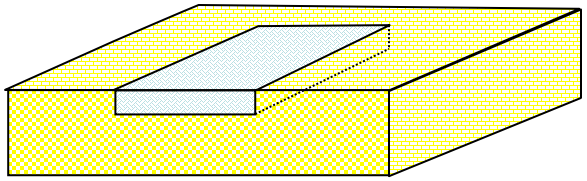
pn junction capacitance

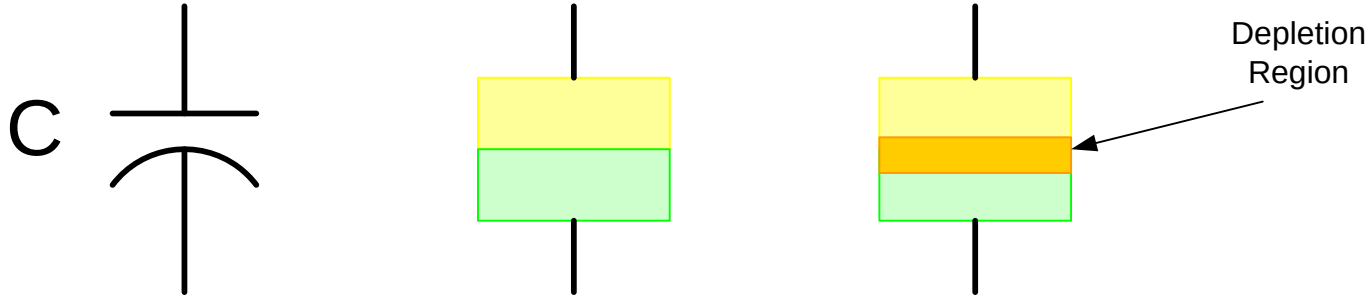


The bottom and the sidewall:

Parasitic Capacitors in MOSFET

pn junction capacitance





For a pn junction capacitor

$$C_J = C_{BOT} A + C_{SW} P$$

$$C_{BOT} = \frac{C_{BOT0}}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m} \qquad C_{SW} = \frac{C_{SW0}}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

A : Junction Area
P: Junction Perimeter
V_{FB}: forward bias on junction

Model Parameters:

$\{C_{BOT0}, C_{SW0}, \varphi_B, m\}$

C_{BOT} and C_{SW} are capacitance densities

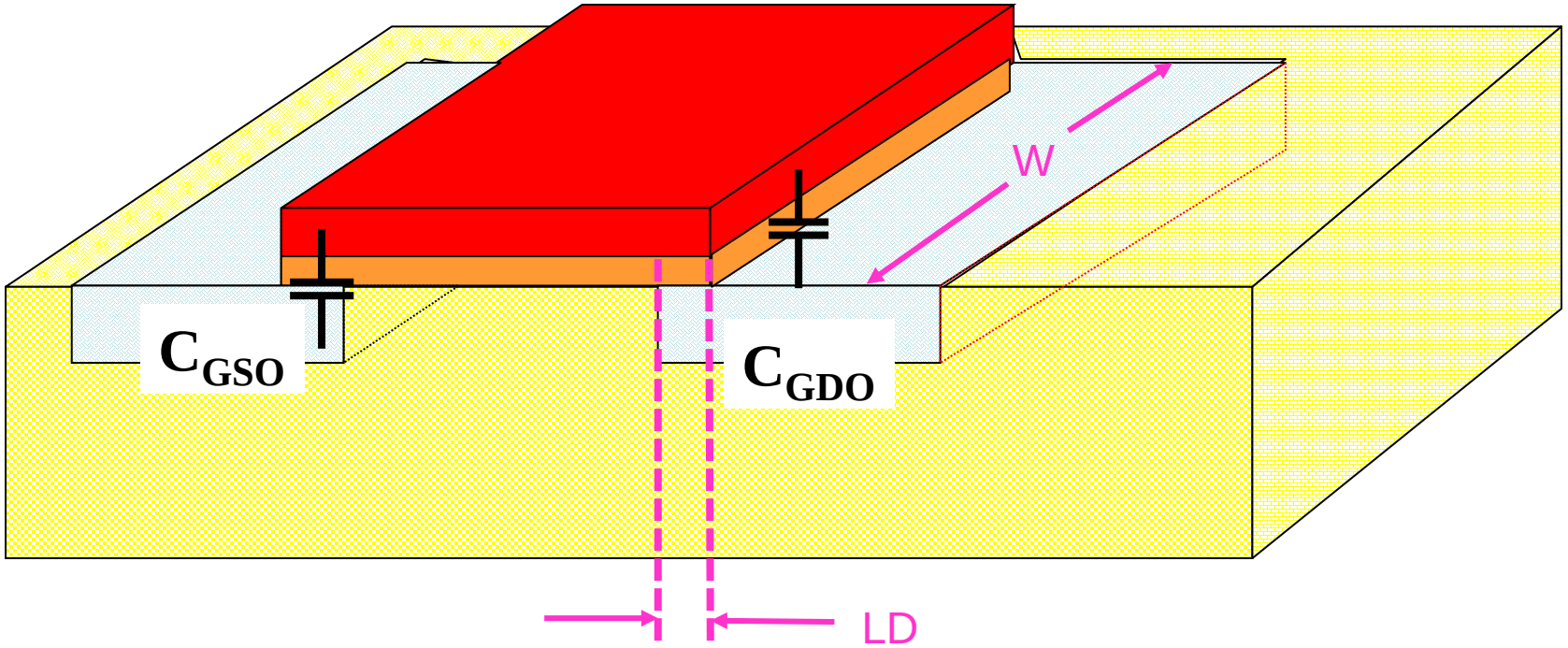
Types of Capacitors in MOSFETs

1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction

2. Operating Region Dependent

Parasitic Capacitors in MOSFET

Fixed Capacitors – Fixed Geometry

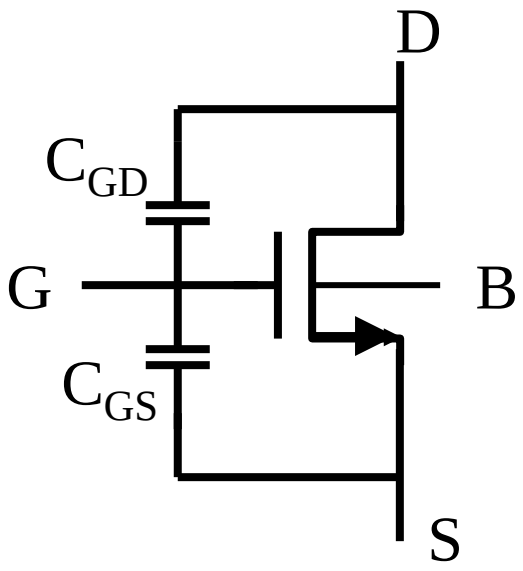


Overlap Capacitors: C_{GDO}, C_{GSO}

Cap Density: C_{OX}

L_D: lateral diffusion

Parasitic Capacitance Summary (partial)



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$

L_D is a model parameter

Overlap Capacitance Model Parameters

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	942	1163	106	34	14	9	6	5	3		123		125	aF/um^2
Area (N+active)			8484	55	20	13	11	9	8					aF/um^2
Area (P+active)			8232											aF/um^2
Area (poly)				66	17	10	7	5	4					aF/um^2
Area (metal1)					37	14	9	6	5					aF/um^2
Area (metal2)						35	14	9	6					aF/um^2
Area (metal3)							37	14	9					aF/um^2
Area (metal4)								36	14					aF/um^2
Area (metal5)									34				984	aF/um^2
Area (r well)	920													aF/um^2
Area (d well)										582				aF/um^2
Area (no well)	137													aF/um^2
Fringe (substrate)	212	235		41	35	29	21	14						aF/um
Fringe (poly)				70	39	29	23	20	17					aF/um
Fringe (metal1)					52	34		22	19					aF/um
Fringe (metal2)						48	35	27	22					aF/um
Fringe (metal3)							53	34	27					aF/um
Fringe (metal4)								58	35					aF/um
Fringe (metal5)									55					aF/um
Overlap (N+active)			895											aF/um
Overlap (P+active)			737											aF/um

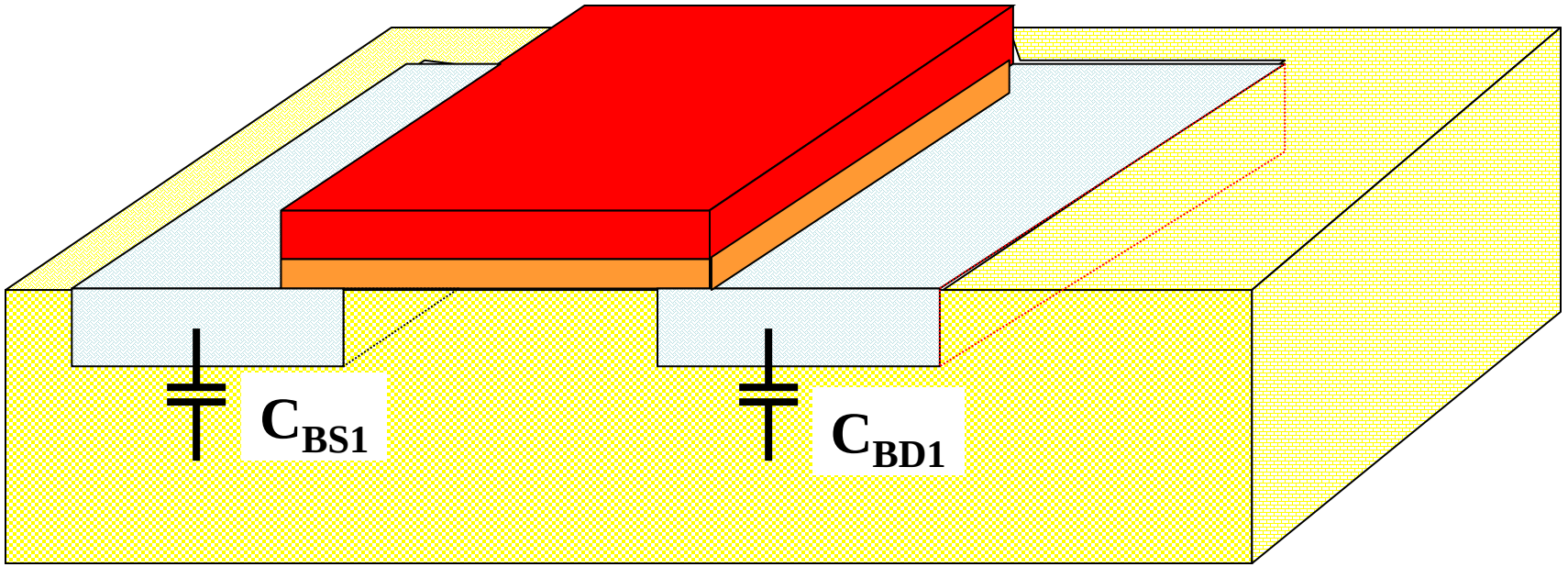
Types of Capacitors in MOSFETs

1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction

2. Operating Region Dependent

Parasitic Capacitors in MOSFET

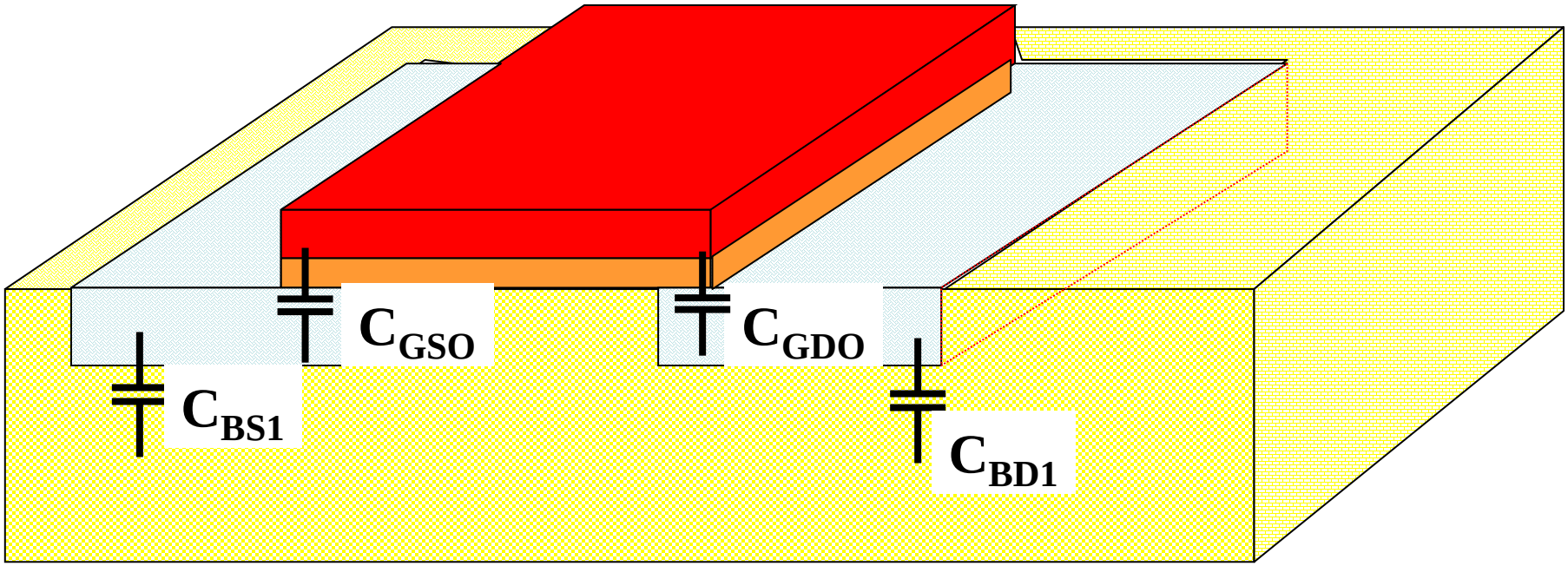
Fixed Capacitors- Junction



Junction Capacitors: C_{BS1}, C_{BD1}

Parasitic Capacitors in MOSFET

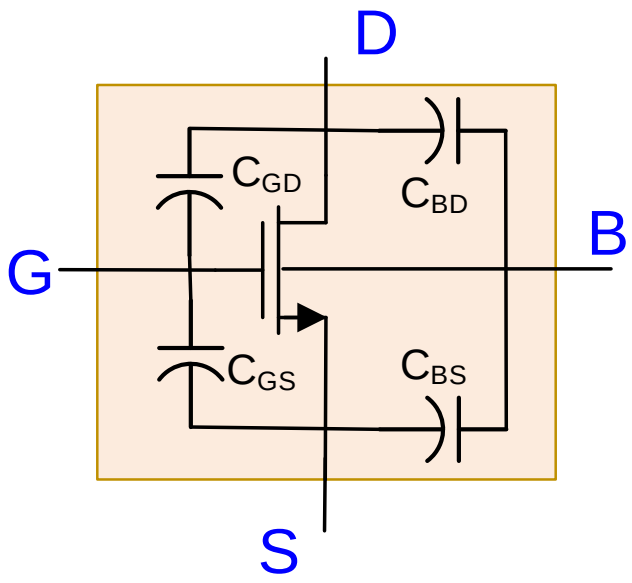
- Fixed Capacitors



Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Fixed Parasitic Capacitance Summary



C_{BOT} and C_{SW} are model parameters

	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{BG}			
C_{BS}	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$
C_{BD}	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$

C_{BOT} and C_{SW} model parameters

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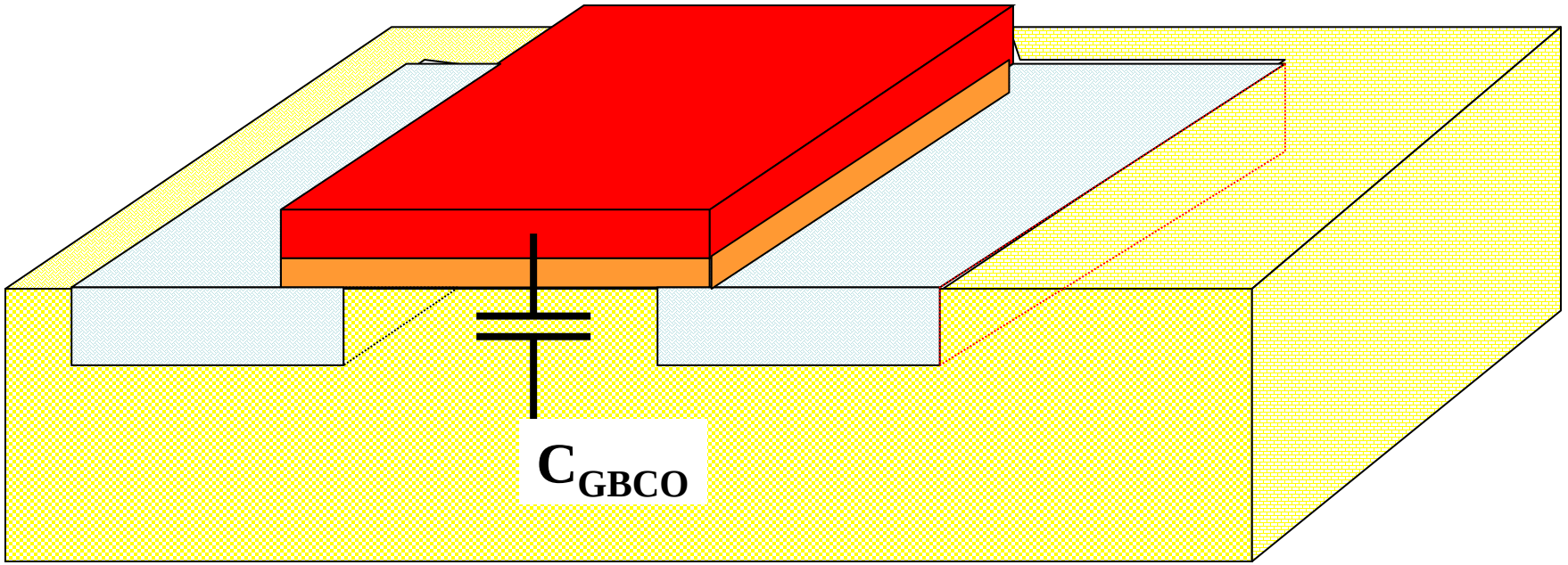
Types of Capacitors in MOSFETs

1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction

2. Operating Region Dependent

Parasitic Capacitors in MOSFET

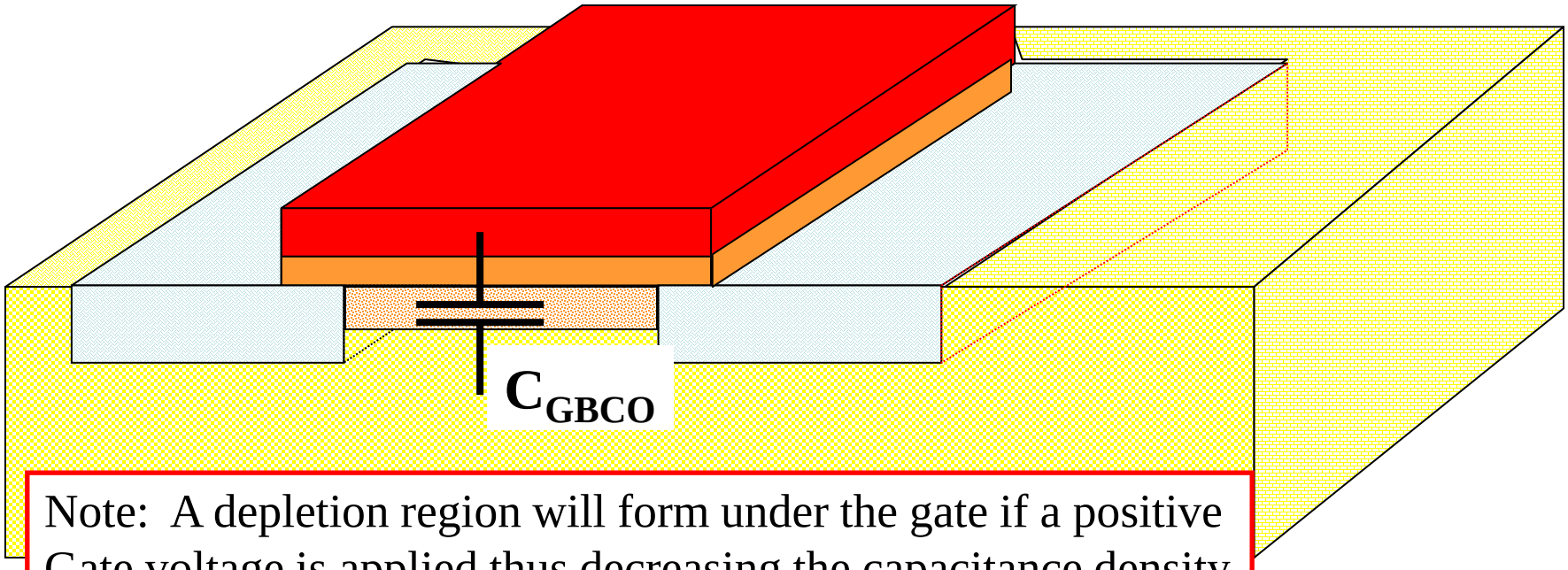
Operation Region Dependent -- Cutoff



Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Cutoff

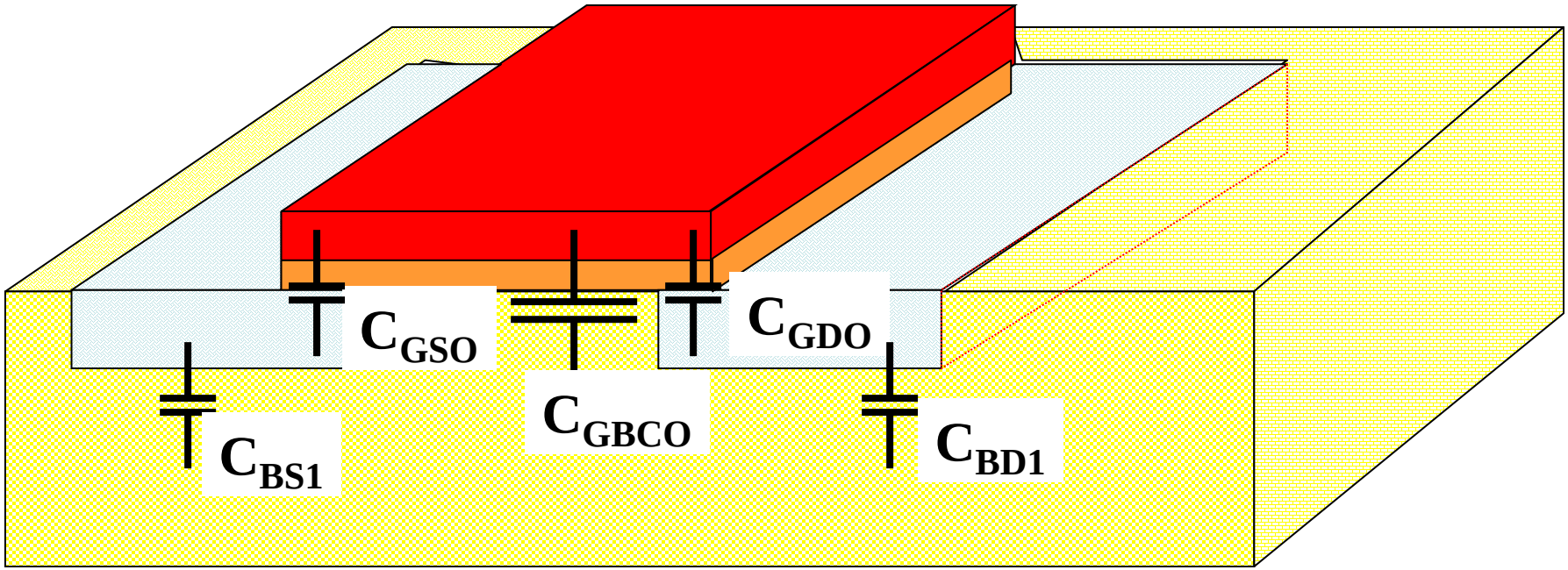


Note: A depletion region will form under the gate if a positive Gate voltage is applied thus decreasing the capacitance density

Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Cutoff

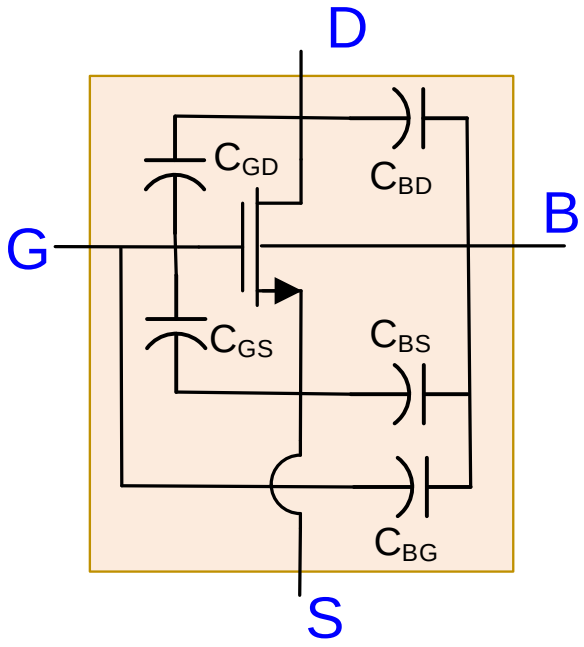


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Cutoff Capacitor: C_{GBCO}

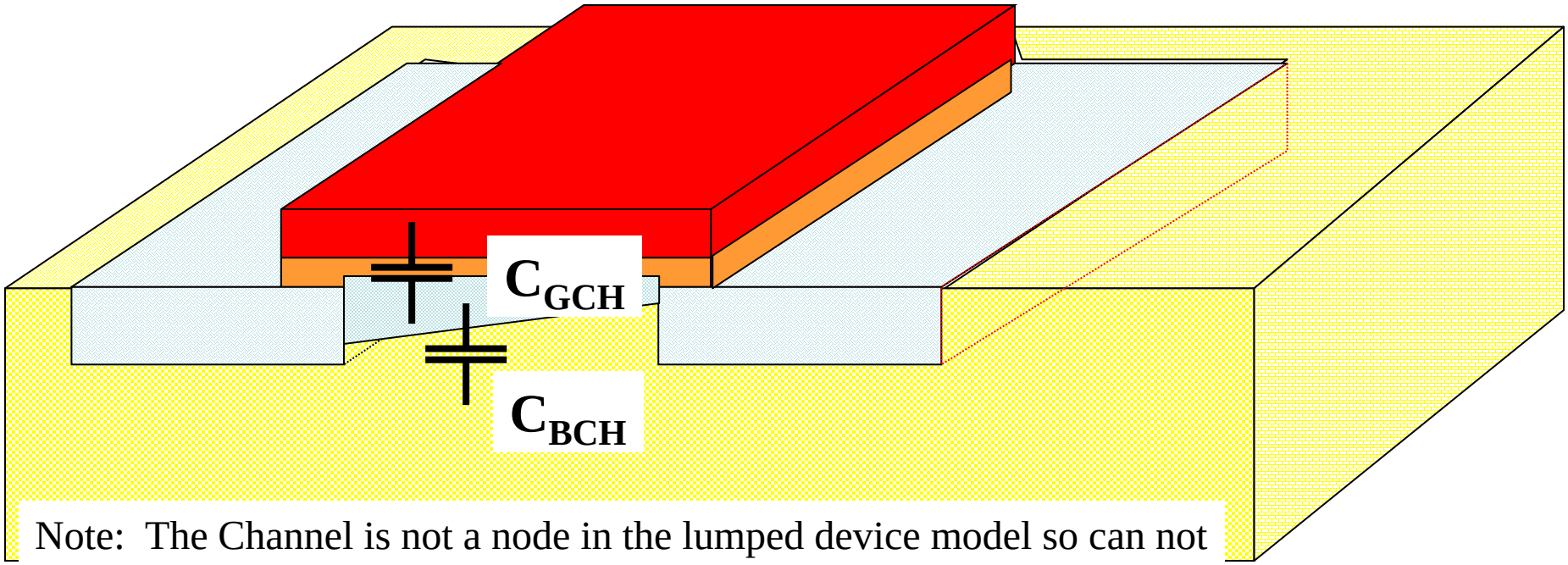
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$		
C_{GD}	$CoxWL_D$		
C_{BG}	CoxWL (or less)		
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$		
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$		

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Ohmic



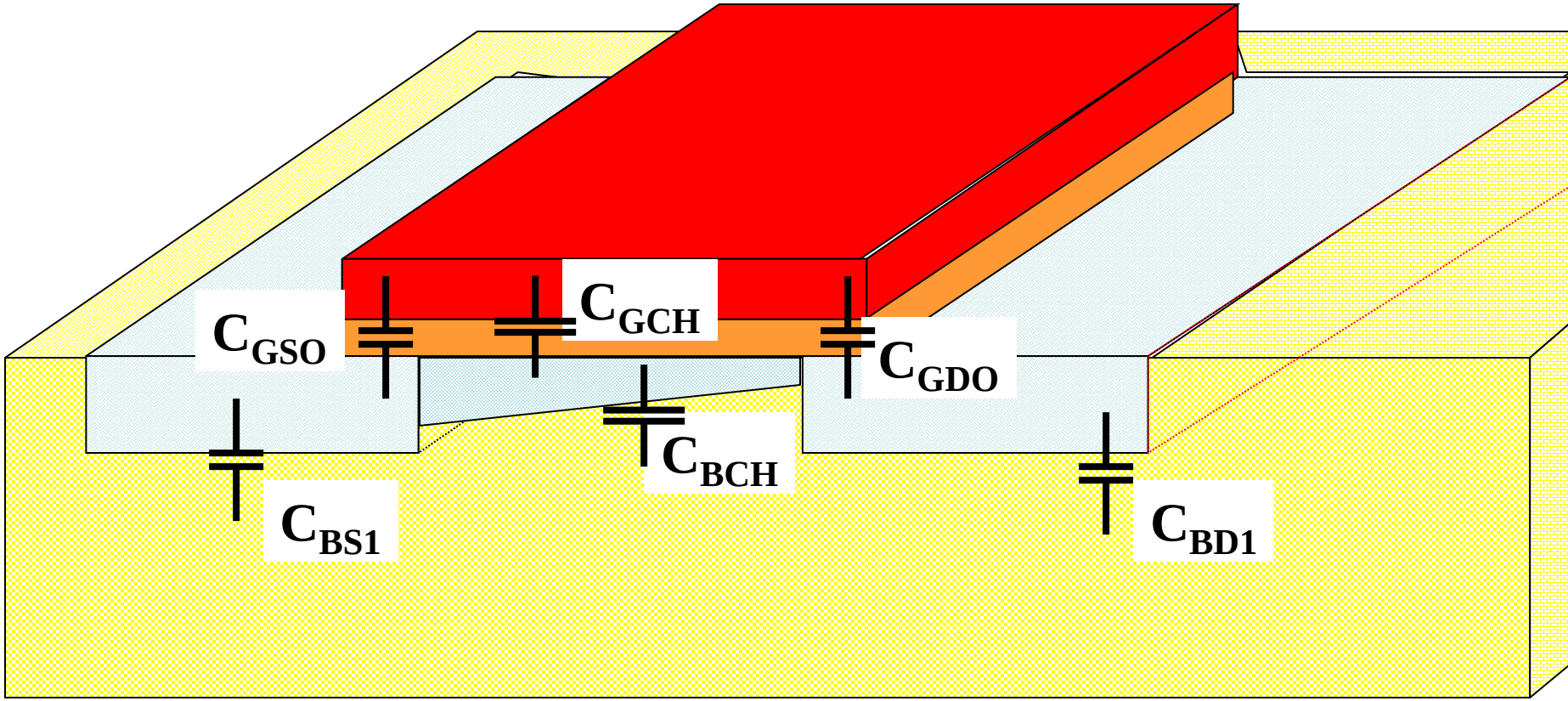
Note: The Channel is not a node in the lumped device model so can not directly include this distributed capacitance in existing models

Note: The distributed channel capacitance is usually lumped and split evenly between the source and drain nodes

Ohmic Capacitor: C_{GCH}, C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Ohmic

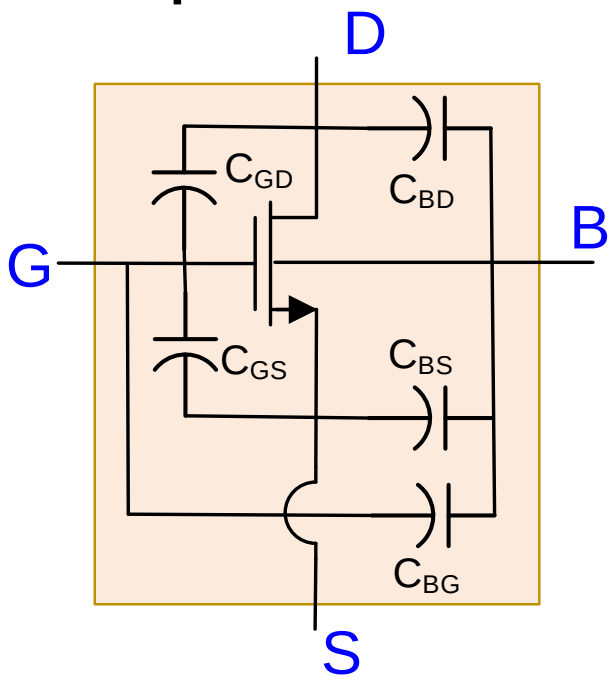


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Ohmic Capacitor: C_{GCH}, C_{BCH}

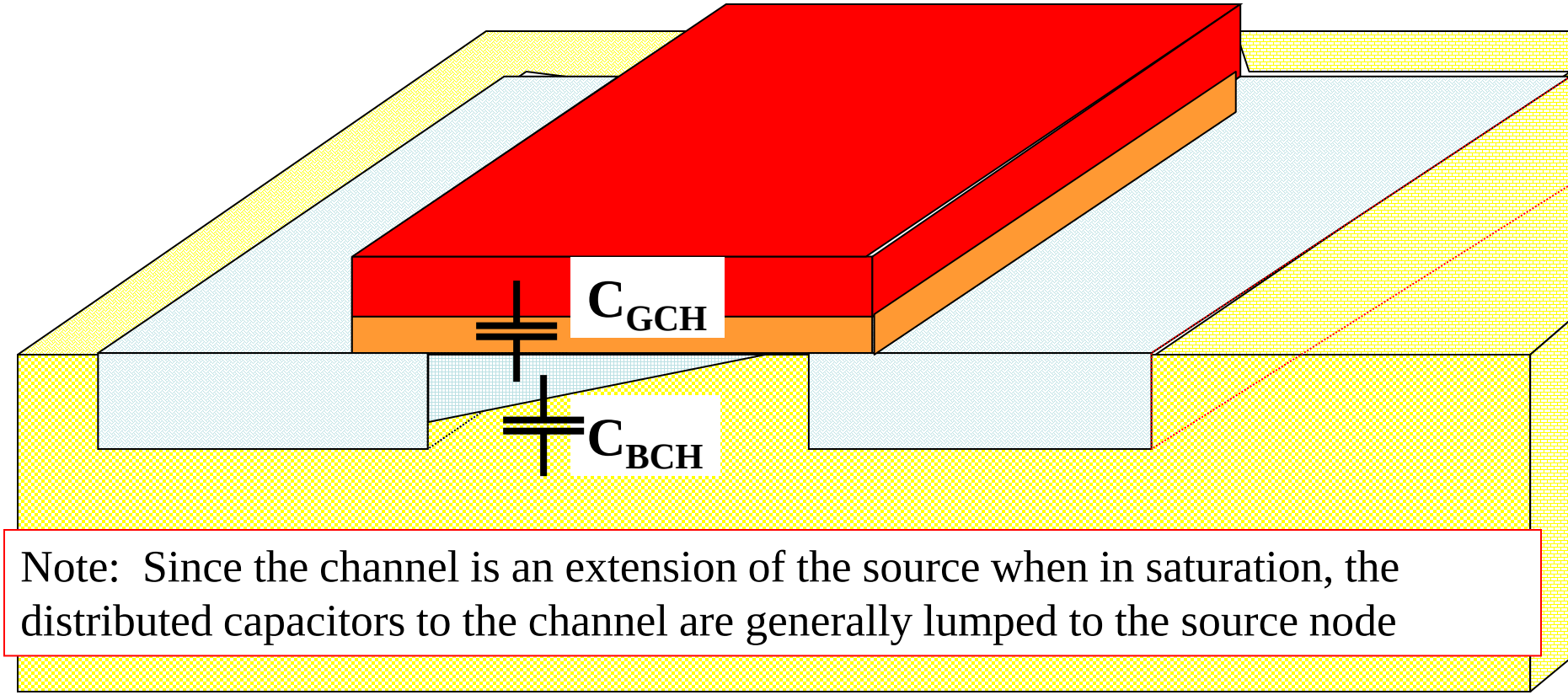
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	0.5CoxWL	
C_{GD}	$CoxWL_D$	0.5CoxWL	
C_{BG}	CoxWL (or less)	0	
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Saturation

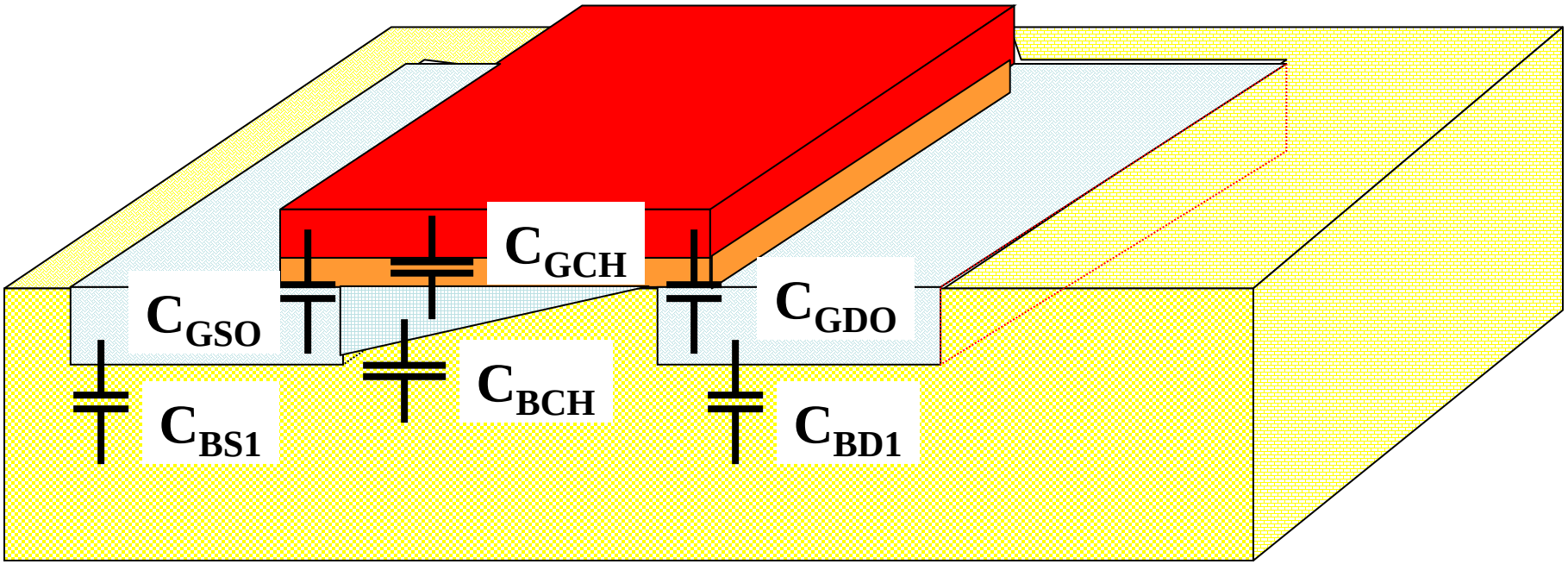


Note: Since the channel is an extension of the source when in saturation, the distributed capacitors to the channel are generally lumped to the source node

Saturation Capacitors: C_{GCH}, C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed --Saturation



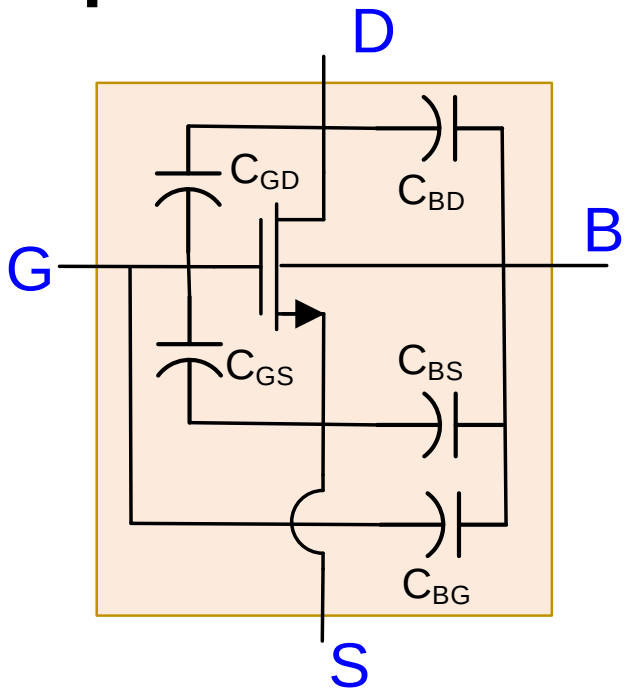
Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Saturation Capacitors: C_{GCH} , C_{BCH}

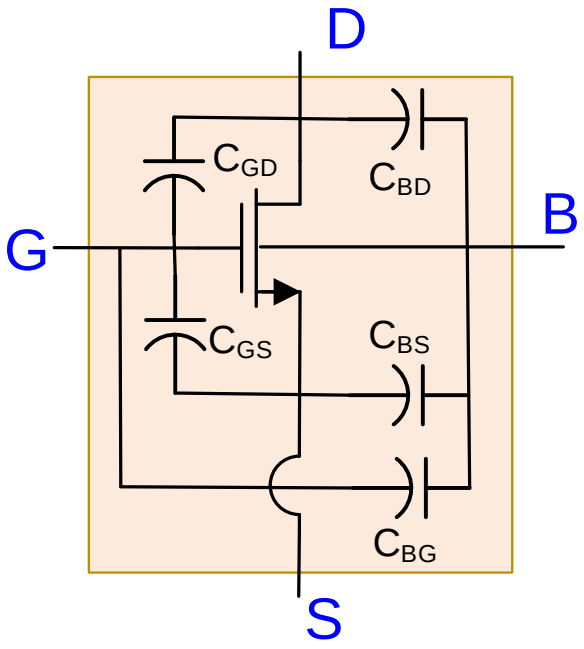
- 2/3 $C_{OX}WL$ is often attributed to C_{GCH} to account for LD and saturation
- This approximation is reasonable for minimum-length devices but not so good for longer devices

Parasitic Capacitance Summary



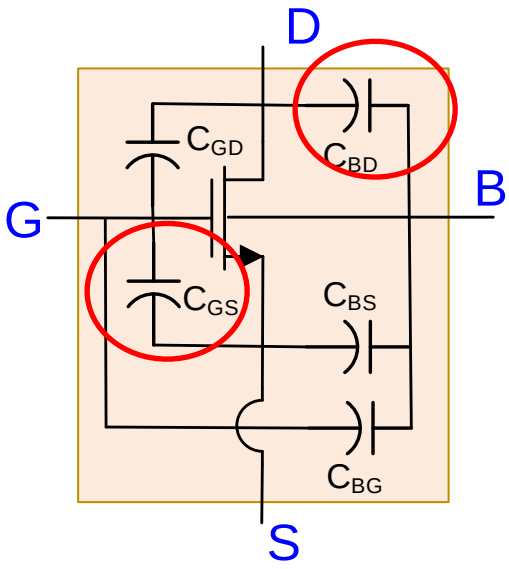
	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S+(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S+(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

Parasitic Capacitance Implications

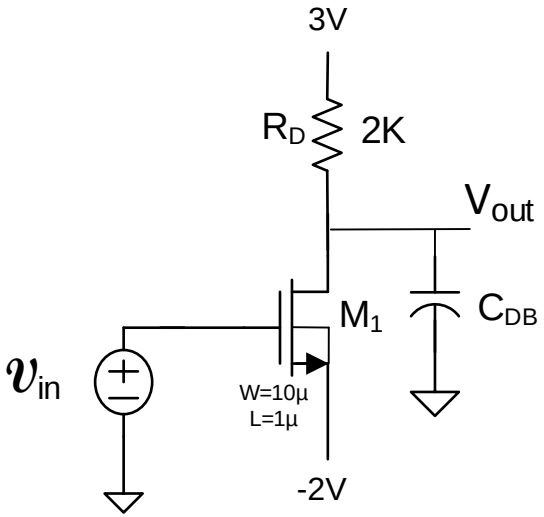


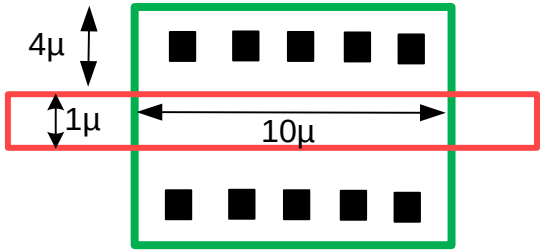
The parasitic capacitances inherently introduce an upper limit on how fast either digital circuits or analog circuits can operate in a given process

Two parameters, f_{MAX} and f_T, (not defined here) are two metric that are used to specify the fundamental speed limit in a semiconductor process

The dominant parasitic capacitances for most circuits are C_{GS} and C_{BD}

Example: Determine the small-signal voltage gain and the 3dB bandwidth. Consider only the effects of C_{DB} on the BW. Assume a 0.5u process with V_{TH}=0.75V and the layout of the transistor shown.





$C_{DB}=C_{BOT}*40u^2+C_{SW}*28u$

$C_{BOT}=942aF/u^2 \quad C_{SW}=212aF/u$

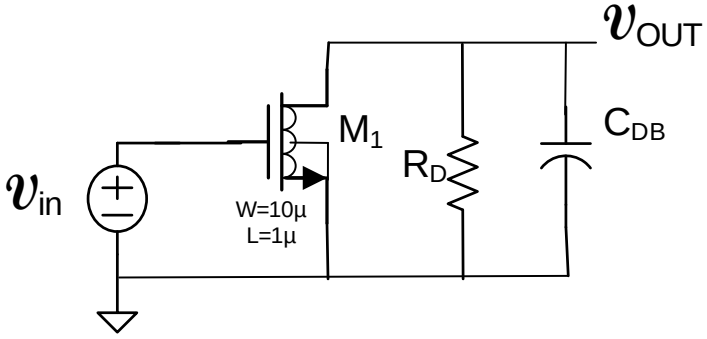
$C_{DB}=942aF/u^2*40u^2+212aF/u*28u$

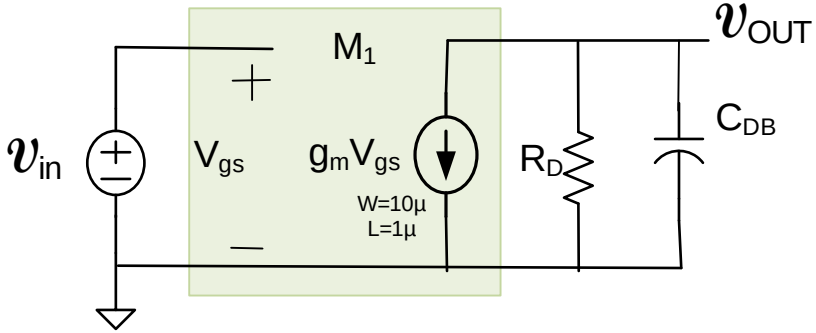
$C_{DB}=37.7fF+5.9fF=43.6fF$

Solution:

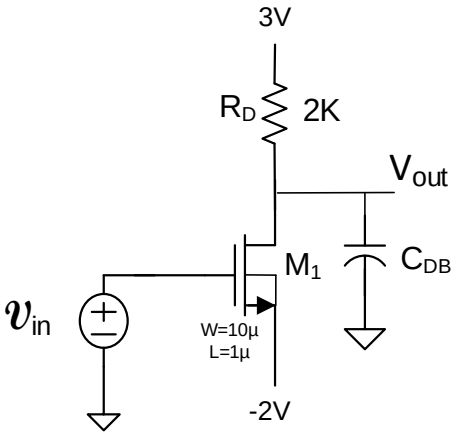
$$I_{DQ}=100\mu A/V^2\frac{10}{2\bullet 1}(2-0.75)^2=0.78mA$$

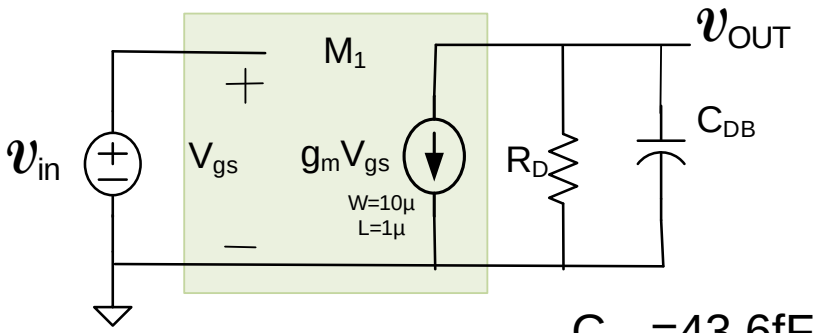
$$I_{DQ}R_D=0.78mA\bullet 2K=1.56$$





Example: Determine the small-signal dc voltage gain and the 3dB bandwidth. Consider only the effects of C_{DB} on the BW. Assume a 0.5u process with V_{TH}=0.75V and the layout of the transistor shown.





C_{DB}=43.6fF

Solution continued:

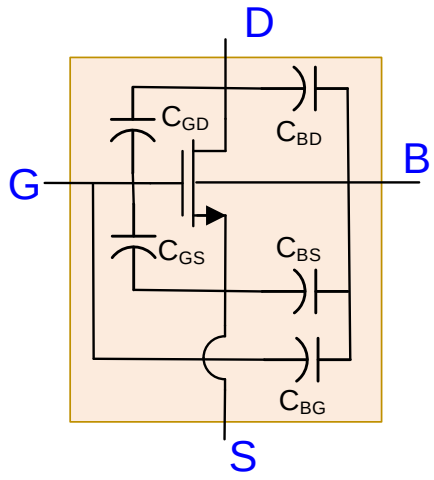
$$v_{OUT}\left(G_D + sC_{DB}\right) + g_m v_{IN} = 0$$

$$v_{OUT} = -v_{IN}\frac{g_m R_D}{1 + sC_{DB}R_D}$$

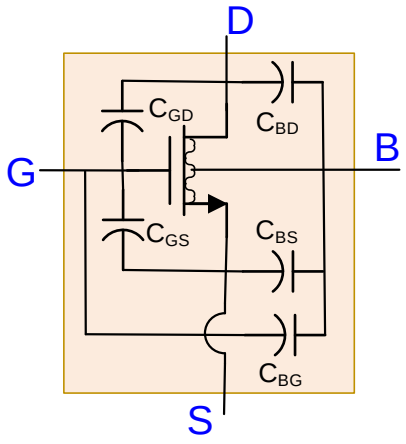
$$A_{V0} = -g_m R_D = -\frac{2I_{DQ}R_D}{V_{EB}} = -\frac{3.12}{1.25} = -2.5$$

$$f_{3dB} = \frac{1}{2\pi} \bullet \frac{1}{R_D C_{DB}} = 1.8GHz$$

Parasitic Capacitance Summary

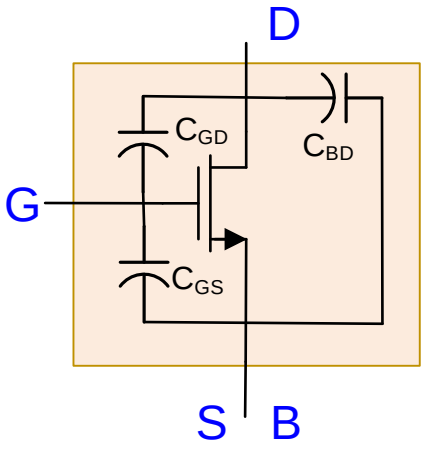


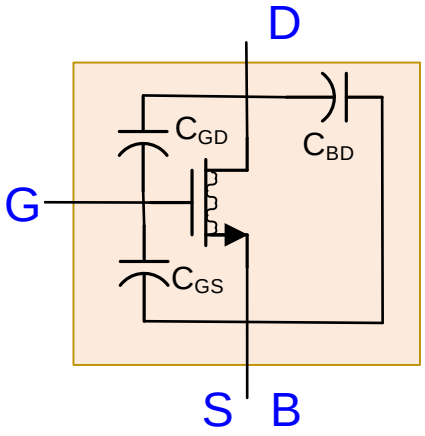
High Frequency Large Signal Model



High Frequency Small Signal Model (saturation region)

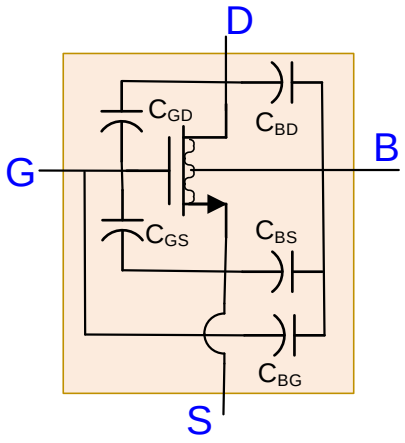
Often V_{BS}=0 and C_{BG}=0 in saturation, so simplifies to

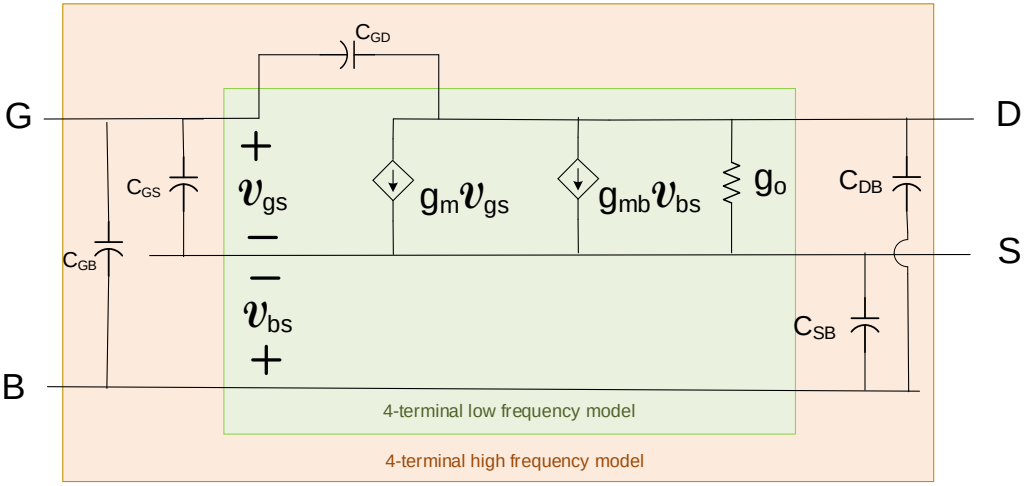




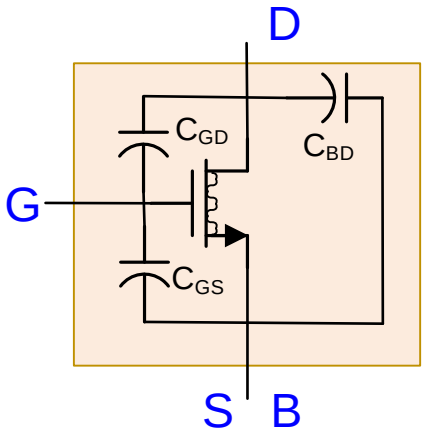
High Frequency Small-Signal Model

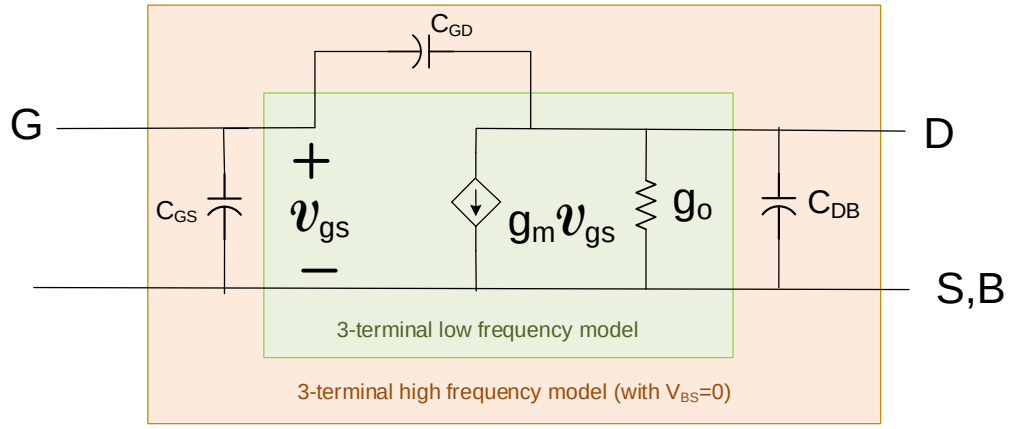
(Saturation Region)





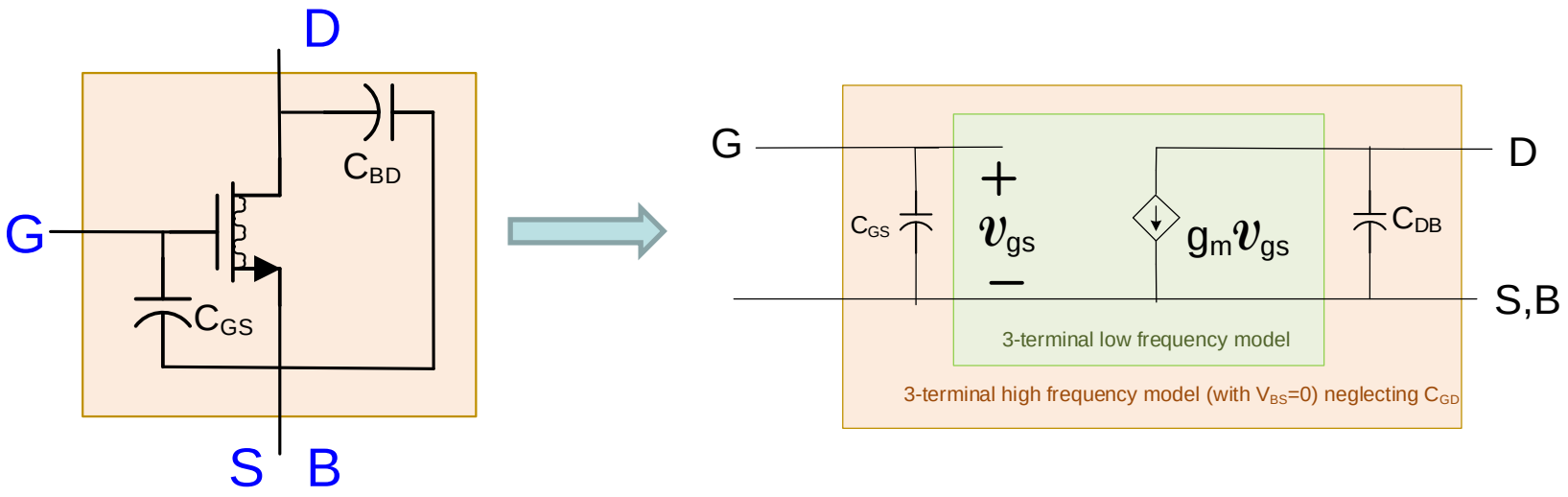
Often V_{BS}=0 and C_{BG}=0, so simplifies to





High Frequency Small-Signal Model

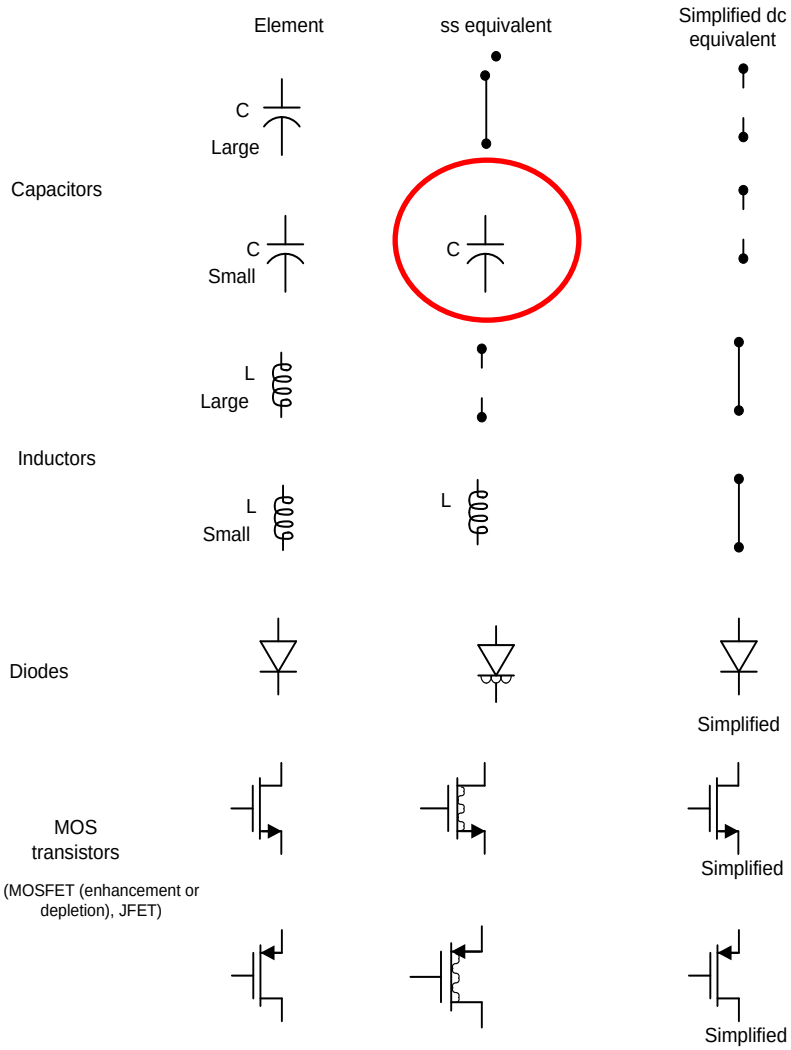
Often $V_{BS}=0$ and $C_{BG}=0$ and C_{GD} and g_0 can be neglected so simplifies farther to



Neglecting C_{GD} which is high frequency feedback from output to input often simplifies analysis considerably

Recall:

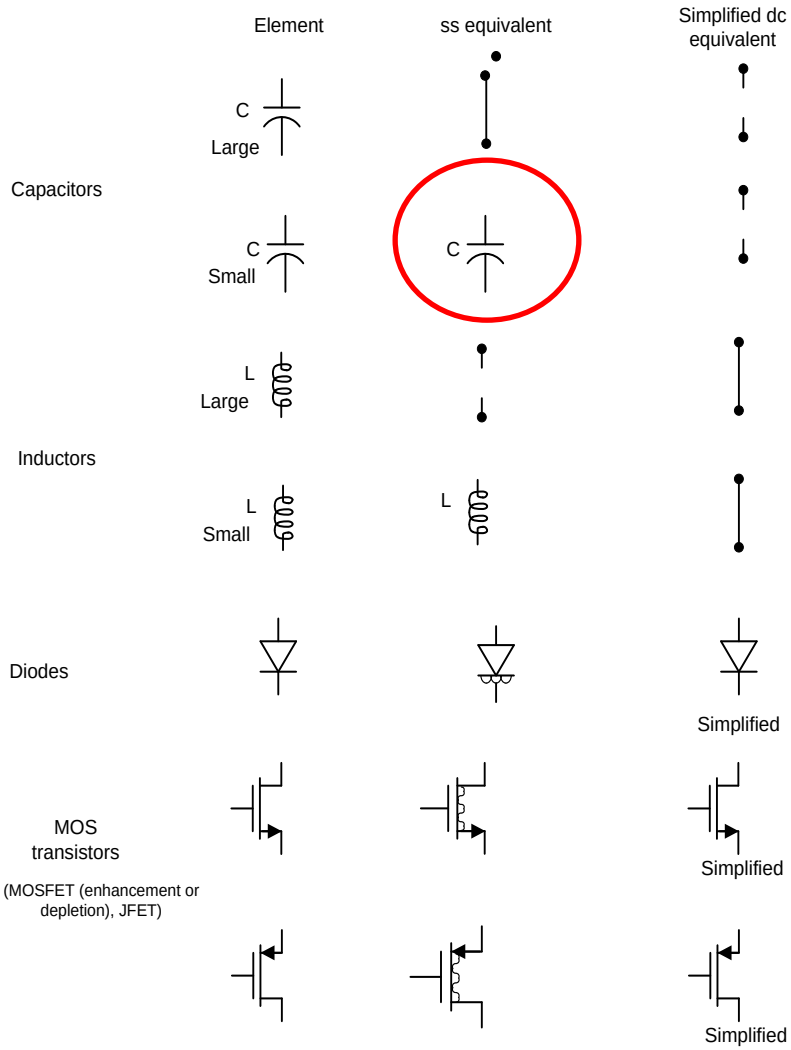
Small-signal and simplified dc equivalent elements



Have not yet considered situations where the small capacitor is relevant in small-signal analysis

Recall:

Small-signal and simplified dc equivalent elements

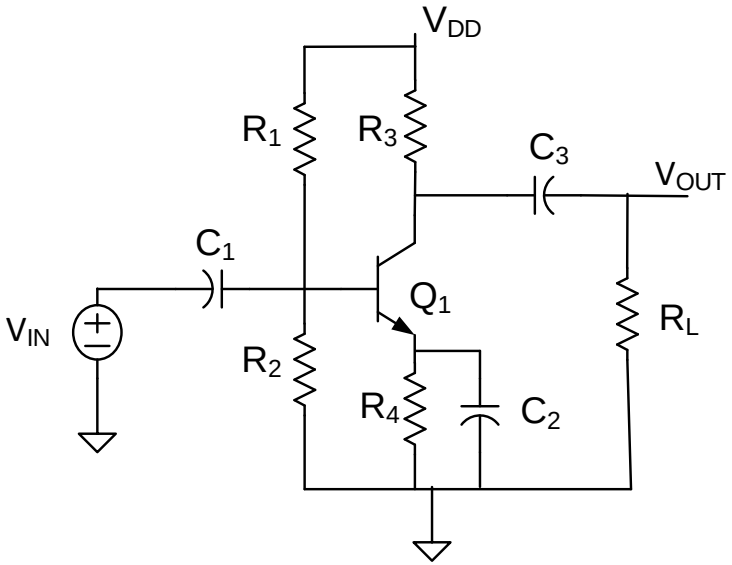


Have not yet considered situations where the small capacitor is relevant in small-signal analysis

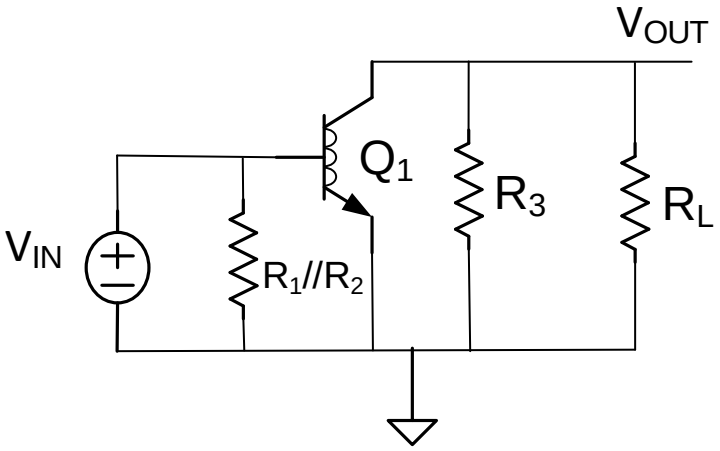
Amplifiers with Small Capacitors

Consider a bipolar amplifier first where C_3 is a small capacitor but not a parasitic capacitor

Recall:



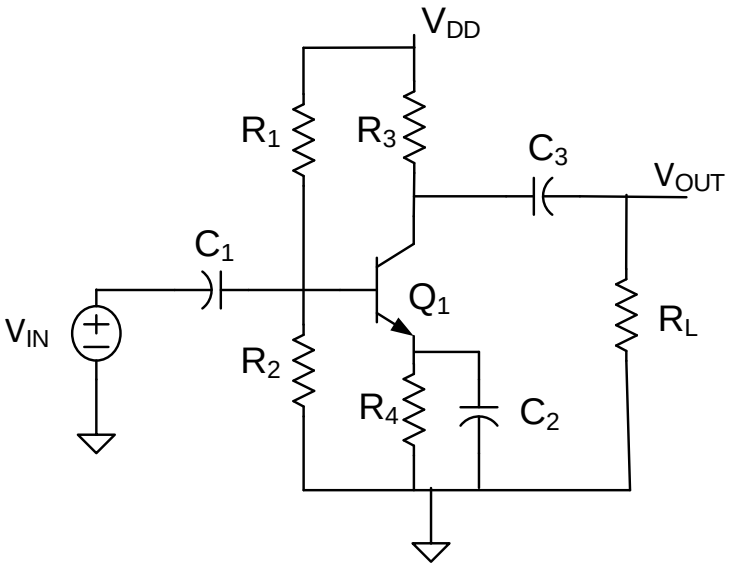
If capacitors are large

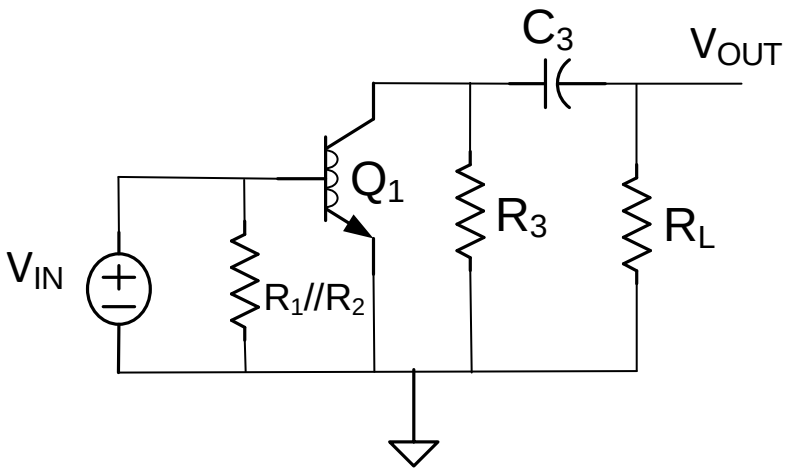


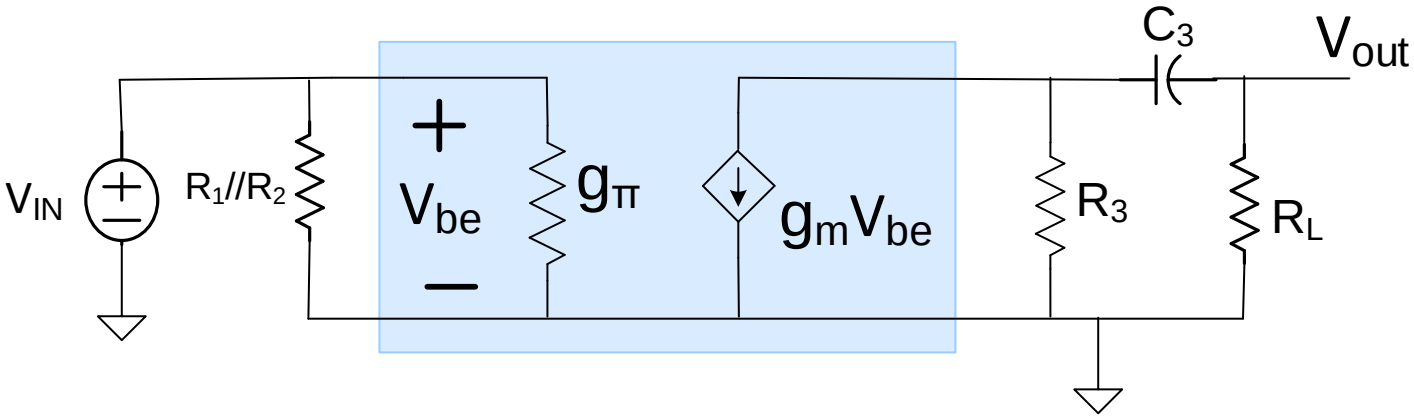
$$A_V = -g_{m1} \bullet R_3 \,//\, R_L$$

Amplifiers with Small Capacitors

What if C_1 and C_2 large but C_3 is not large?:

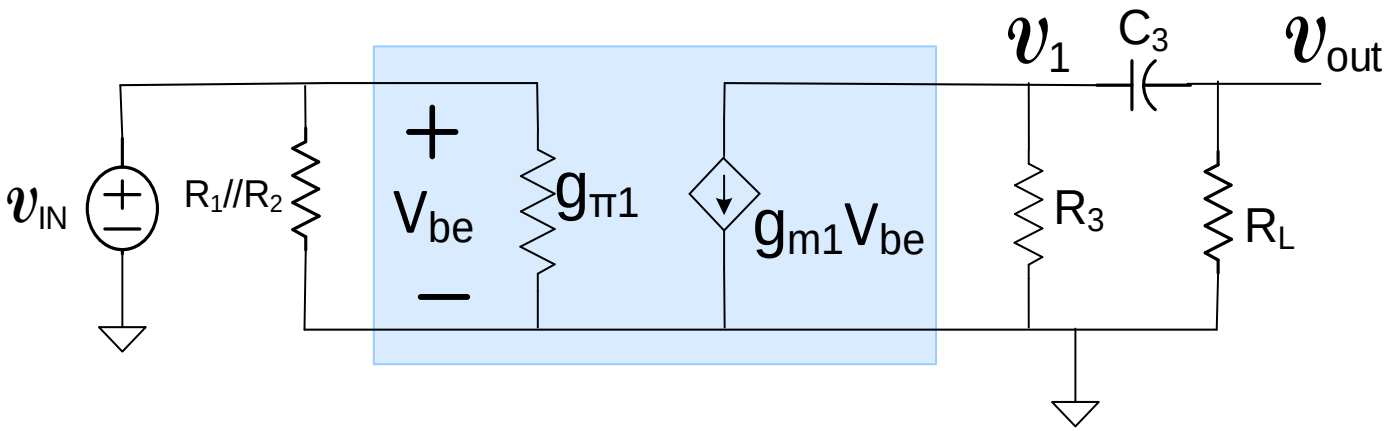






Amplifiers with Small Capacitors

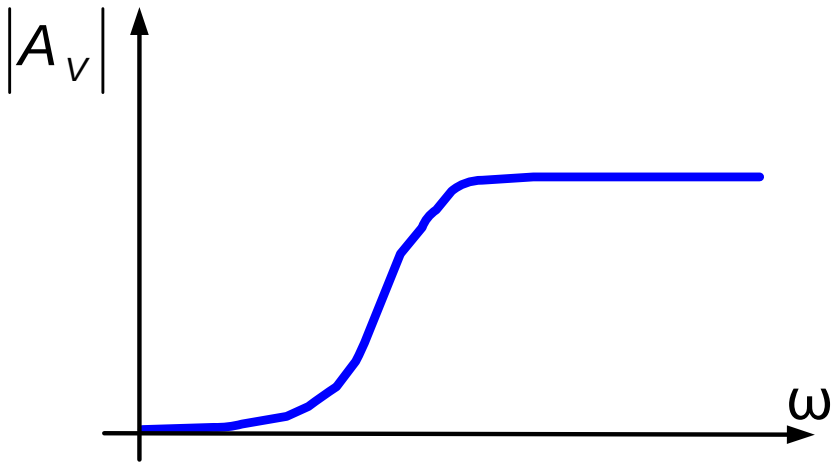
What if C_1 and C_2 large but C_3 not large?:



From KCL:

$$\left.\begin{aligned} v_{OUT}\left(sC_3+G_L\right) &= v_1 sC_3 \\ v_1\left(sC_3+G_3\right)+g_{m1}v_{IN} &= v_{OUT}sC_3 \end{aligned}\right\}$$

Serves as a first-order high-pass filter



Solving:

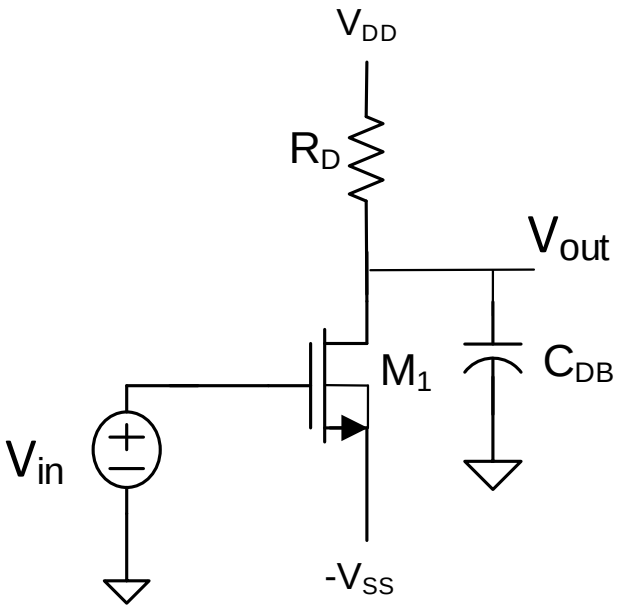
$$\frac{v_{OUT}}{v_{IN}} = -\frac{-sC_3 g_{m1}}{sC_3\left(G_L+G_3\right)+G_3G_L}$$

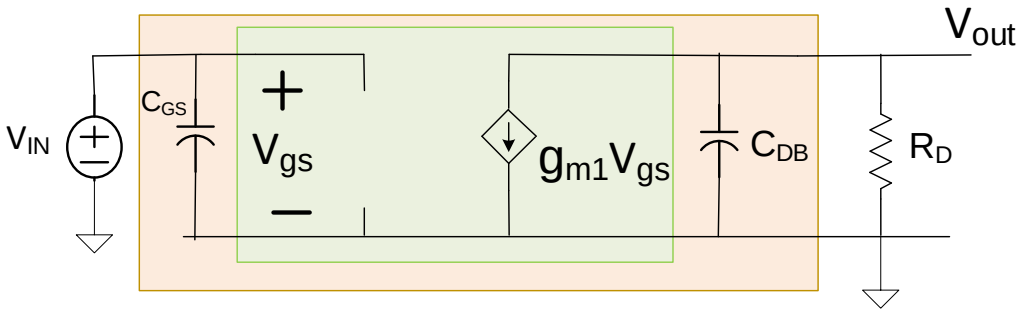
Equivalently:

$$\frac{v_{OUT}}{v_{IN}} = -\frac{g_{m1}sC_3R_3R_L}{sC_3\left(R_L+R_3\right)+1}$$

Amplifiers with Small Capacitors

Consider parasitic C_{GS} and C_{DB}





By KCL:

$$v_{OUT}\left(sC_{DB}+G_D\right)=-g_{m1}v_{IN}$$

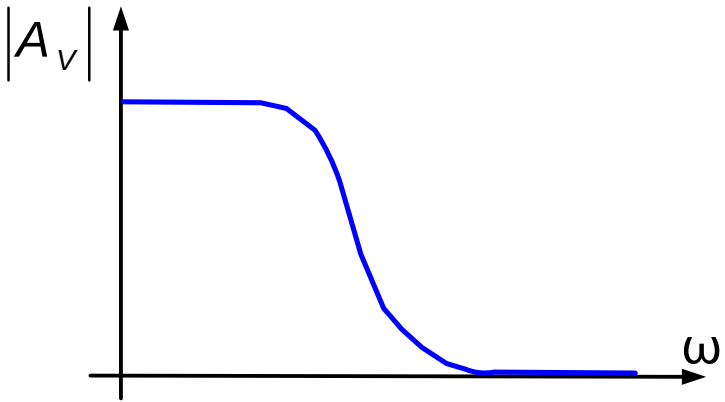
Causes gain to decrease at high frequencies

Solving:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-g_{m1}}{sC_{DB}+G_D}$$

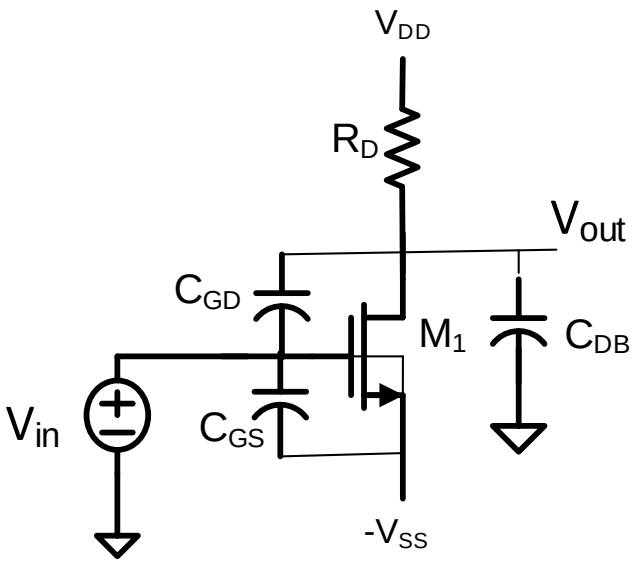
Equivalently:

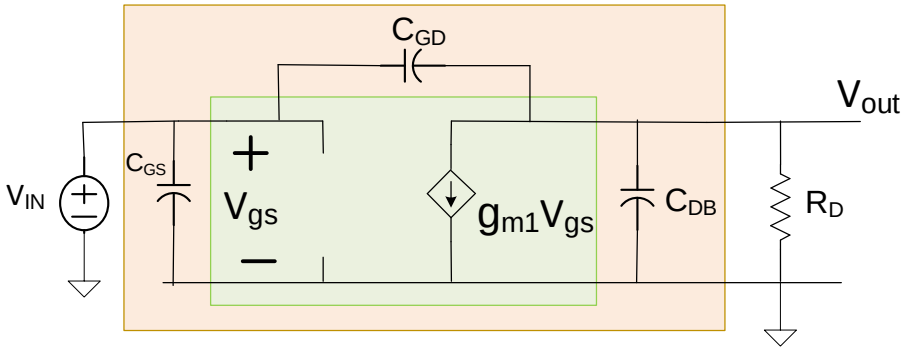
$$\frac{v_{OUT}}{v_{IN}}=-\frac{-g_{m1}R_D}{sC_{DB}R_D+1}$$



Amplifiers with Small Capacitors

Consider parasitic C_{GS}, C_{GD}, and C_{DB}





By KCL:

$$v_{OUT}\left(s\left[C_{DB}+C_{GD}\right]+G_D\right)=-g_{m1}v_{IN}+sC_{GD}v_{IN}$$

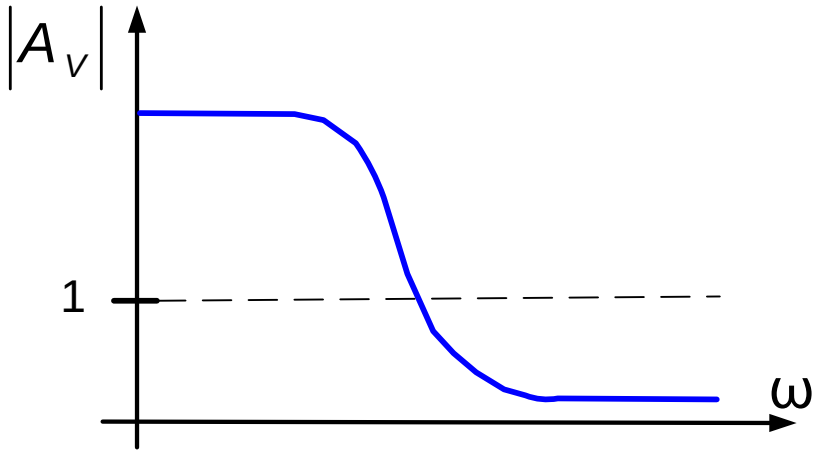
Causes gain to decrease at high frequencies
Has one LHP pole and one RHP zero

Solving:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-g_{m1}+sC_{GD}}{s\left[C_{DB}+C_{GD}\right]+G_D}$$

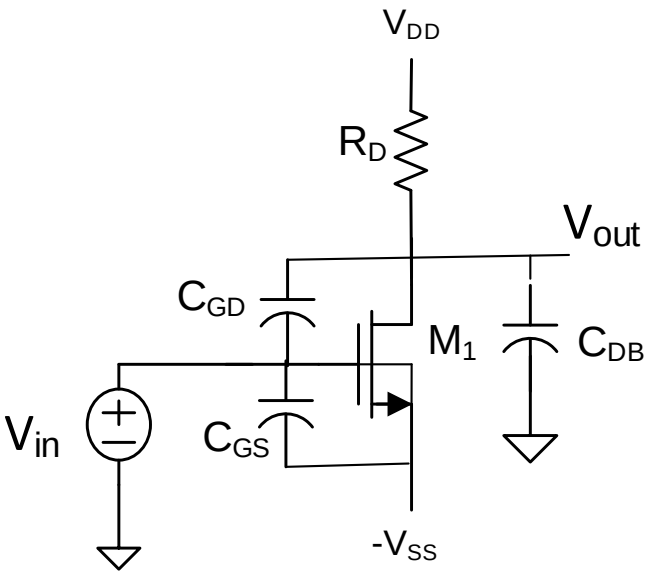
Equivalently:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-R_D\left(g_{m1}-sC_{GD}\right)}{s\left[C_{DB}+C_{GD}\right]R_D+1}$$



Amplifiers with Small Capacitors

Consider parasitic C_{GS}, C_{GD}, and C_{DB}



Device parasitics problematic at high frequencies

C_{DB}, C_{GD} and C_{GS} effects can be significant

Value of parasitic capacitances strongly dependent upon layout

Device parasitics usually not a problem at audio frequencies

Causes gain to decrease at high frequencies:
has one high frequency LHP pole and one high frequency RHP zero.

Stay Safe and Stay Healthy !

End of Lecture 35